Revision History

Version	Date	By	Change Description	Approved
V2	2026-06-05	Xiangwy	合并电源	
V2.1	2026-07-21	Xiangwy	修改AU4562 EN电路, 更新K3 Symbol	

SPACEMIT 进迭时空

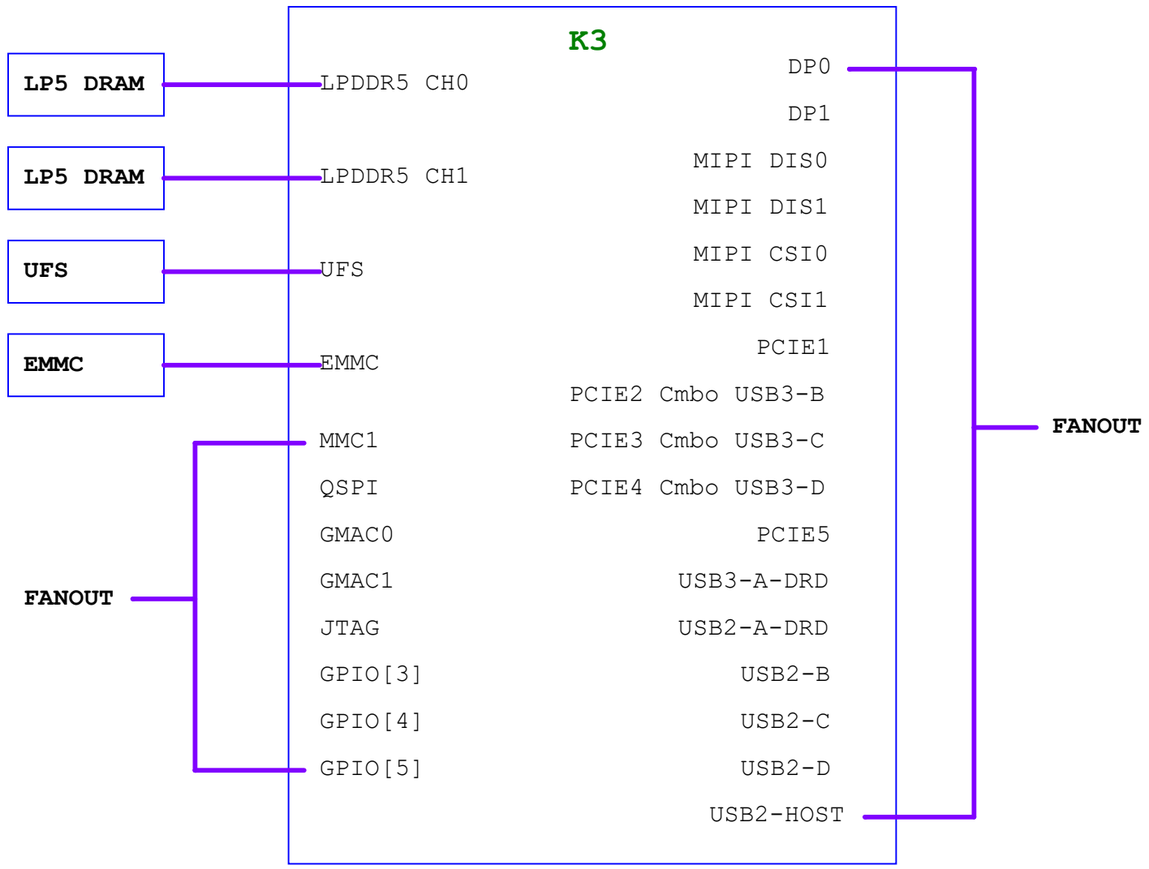
Document Number <Doc>		
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 1 of 29	

Table of Content

SPACEMIT 进迭时空

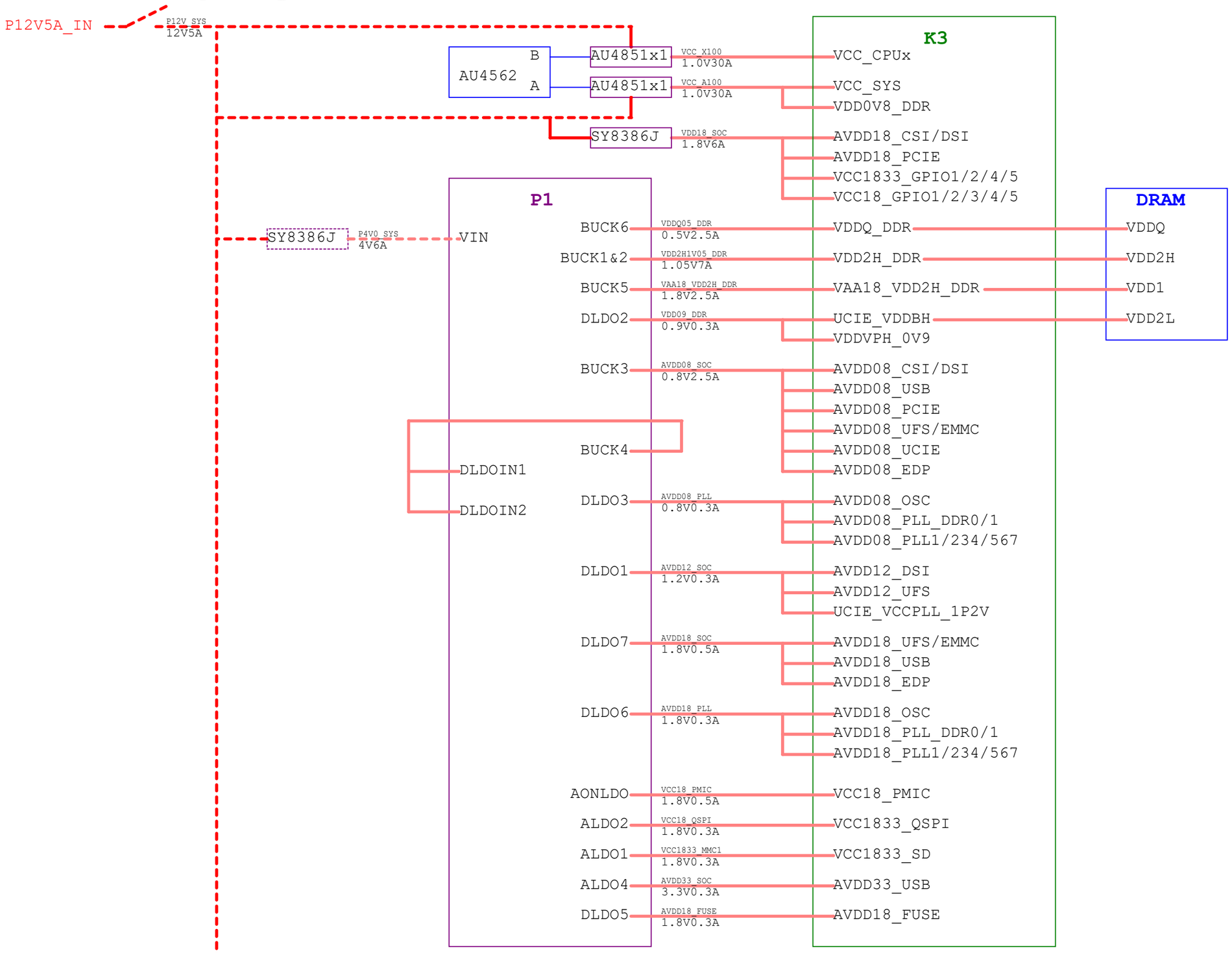
Document Number <Doc>		
Size A3	Title <Title>	Rev A
Date: Tuesday, June 16, 2026	Sheet 2 of 29	

System Block Diagram



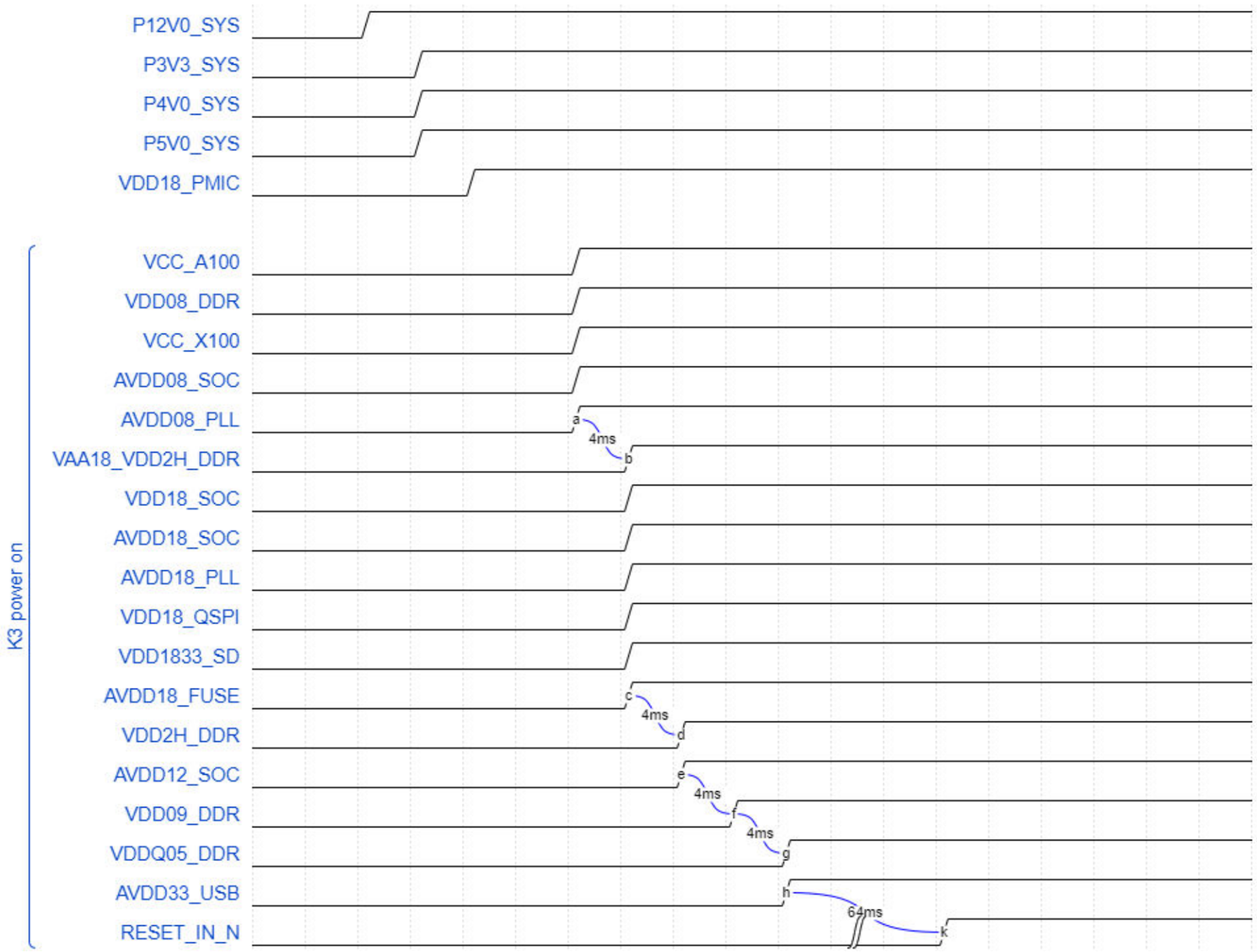
Document Number	<Doc>	
Size A3	Title <Title>	Rev A
Date: Tuesday, June 16, 2026	Sheet 3 of 29	

Power Delivery Diagram



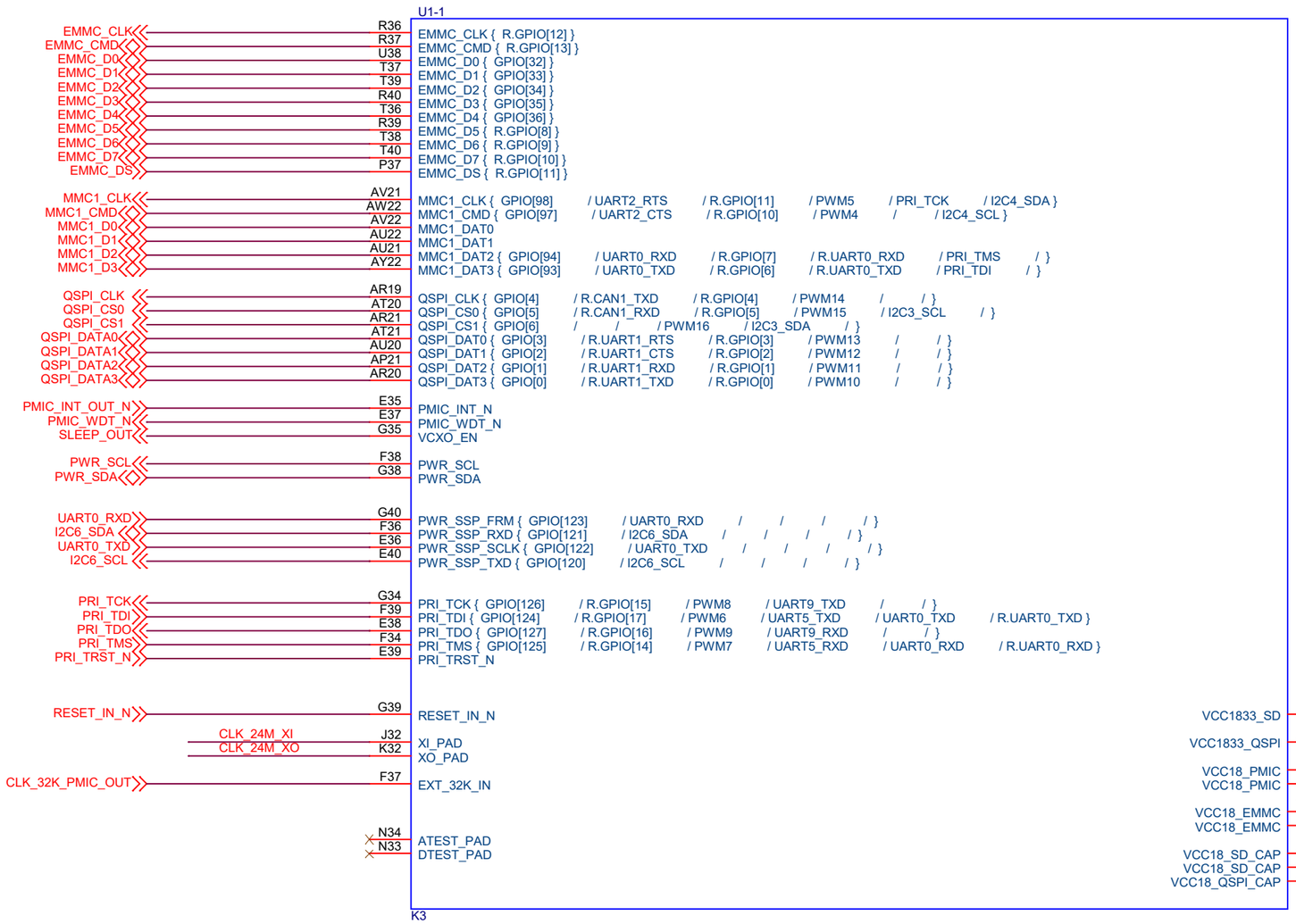
Document Number	<Doc>	
Size A3	Title <Title>	Rev A
Date: Tuesday, June 16, 2026	Sheet 4 of 29	

Power Sequence Diagram



SPACEMIT 进迭时空		
Document Number <Doc>		
Size A3	Title <Title>	Rev A
Date: Tuesday, June 16, 2026	Sheet 5 of 29	

K3-MMC1&JTAG&MISC



SPACEMIT 进迭时空

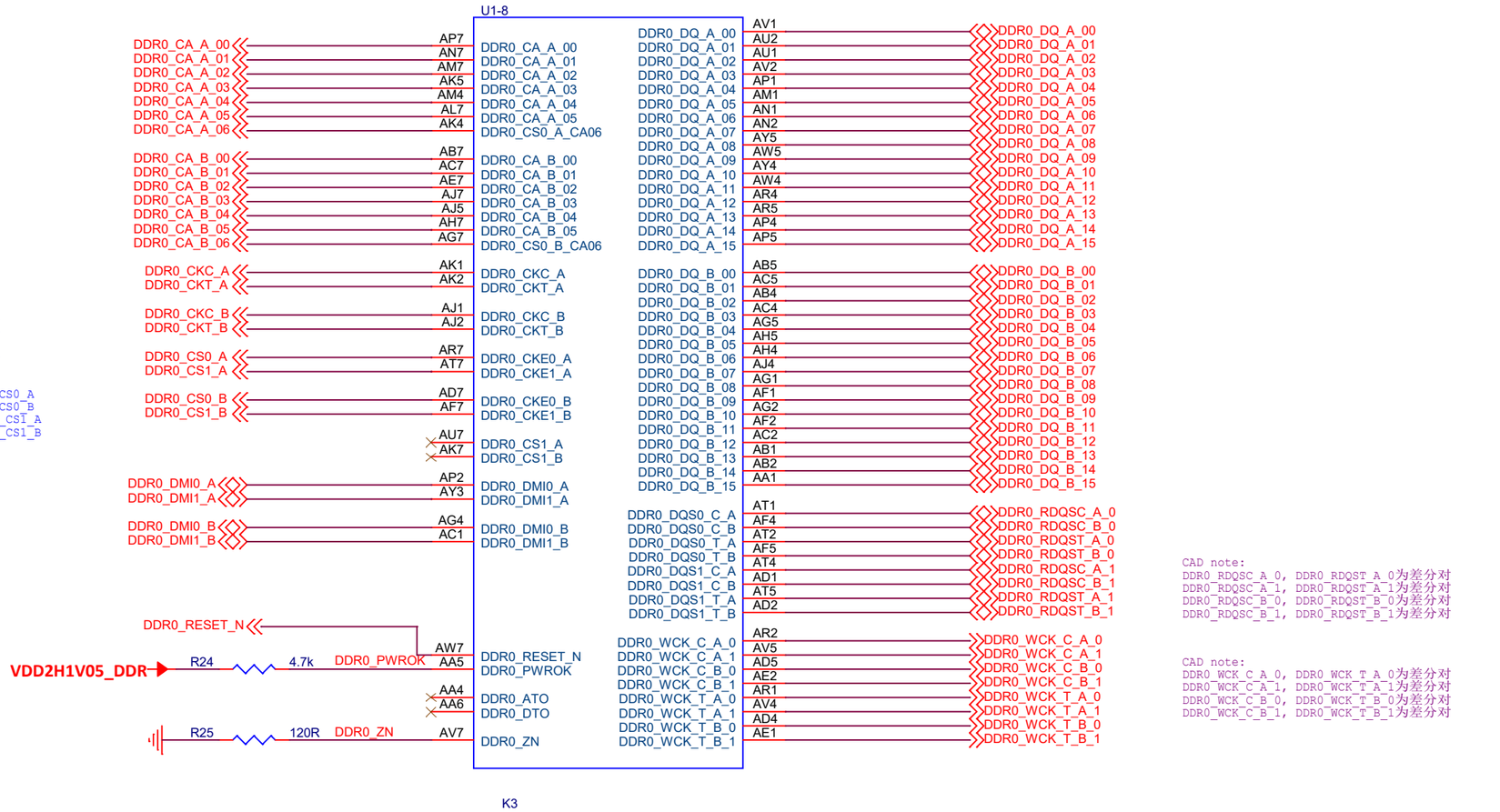
Document Number <Doc>		
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 6 of 29	

K3-DDR CH0

Design note:
DDR0&DDR0 LP5/LP4 Pin 复用如下

DDR0_CKE0_A	LP5_DDR0_CS0_A	LP4_DDR0_CKE0_A
DDR0_CKE0_B	LP5_DDR0_CS0_B	LP4_DDR0_CKE0_B
DDR0_CKE1_A	LP5_DDR0_CS1_A	LP4_DDR0_CKE1_A
DDR0_CKE1_B	LP5_DDR0_CS1_B	LP4_DDR0_CKE1_B

DDR0_CS0_A_CA06	LP5_DDR0_CA_A_06	LP4_DDR0_CS0_A
DDR0_CS0_B_CA06	LP5_DDR0_CA_B_06	LP4_DDR0_CS0_B
DDR0_CS1_A	NA	LP4_DDR0_CS1_A
DDR0_CS1_B	NA	LP4_DDR0_CS1_B



CAD note:
DDR0_RDQSC_A_0, DDR0_RDQST_A_0为差分对
DDR0_RDQSC_A_1, DDR0_RDQST_A_1为差分对
DDR0_RDQSC_B_0, DDR0_RDQST_B_0为差分对
DDR0_RDQSC_B_1, DDR0_RDQST_B_1为差分对

CAD note:
DDR0_WCK_C_A_0, DDR0_WCK_T_A_0为差分对
DDR0_WCK_C_A_1, DDR0_WCK_T_A_1为差分对
DDR0_WCK_C_B_0, DDR0_WCK_T_B_0为差分对
DDR0_WCK_C_B_1, DDR0_WCK_T_B_1为差分对

SPACEMIT 进迭时空

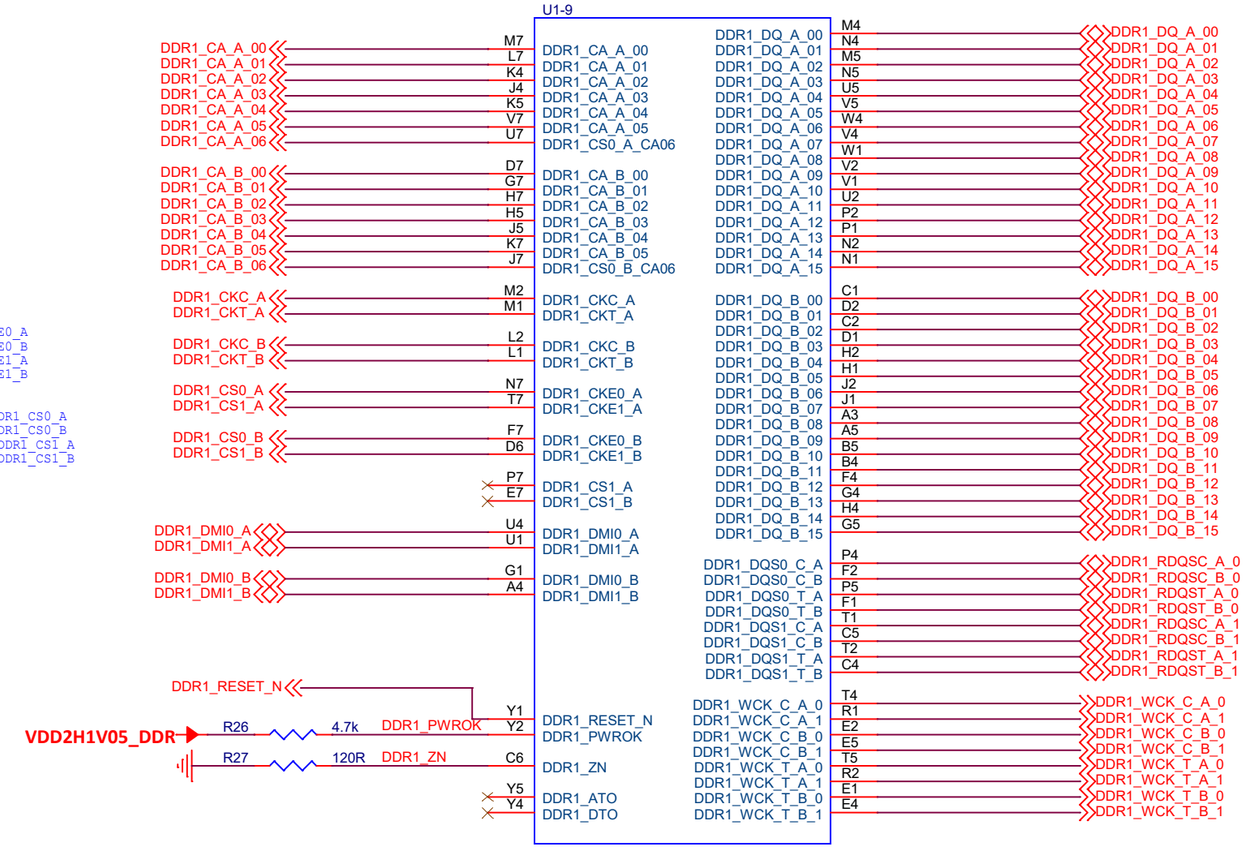
Document Number	<Doc>	
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 7 of 29	

K3-DDR CH1

Design note:
DDR0&DDR1 LP5/LP4 Pin 复用如下

DDR1_CKE0_A	LP5_DDR1_CS0_A	LP4_DDR1_CKE0_A
DDR1_CKE0_B	LP5_DDR1_CS0_B	LP4_DDR1_CKE0_B
DDR1_CKE1_A	LP5_DDR1_CS1_A	LP4_DDR1_CKE1_A
DDR1_CKE1_B	LP5_DDR1_CS1_B	LP4_DDR1_CKE1_B

DDR1_CS0_A_CA06	LP5_DDR1_CA_A_06	LP4_DDR1_CS0_A
DDR1_CS0_B_CA06	LP5_DDR1_CA_B_06	LP4_DDR1_CS0_B
DDR1_CS1_A	NA	LP4_DDR1_CS1_A
DDR1_CS1_B	NA	LP4_DDR1_CS1_B



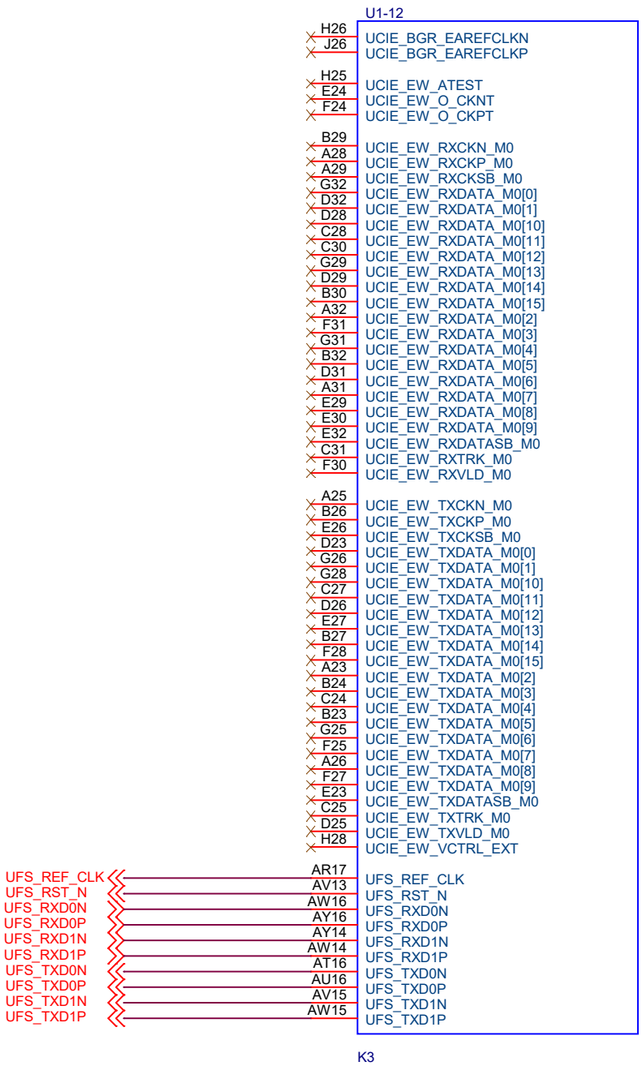
CAD note:
DDR1_RDQSC_A_0, DDR1_RDQST_A_0为差分对
DDR1_RDQSC_A_1, DDR1_RDQST_A_1为差分对
DDR1_RDQSC_B_0, DDR1_RDQST_B_0为差分对
DDR1_RDQSC_B_1, DDR1_RDQST_B_1为差分对

CAD note:
DDR1_WCK_C_A_0, DDR1_WCK_T_A_0为差分对
DDR1_WCK_C_A_1, DDR1_WCK_T_A_1为差分对
DDR1_WCK_C_B_0, DDR1_WCK_T_B_0为差分对
DDR1_WCK_C_B_1, DDR1_WCK_T_B_1为差分对

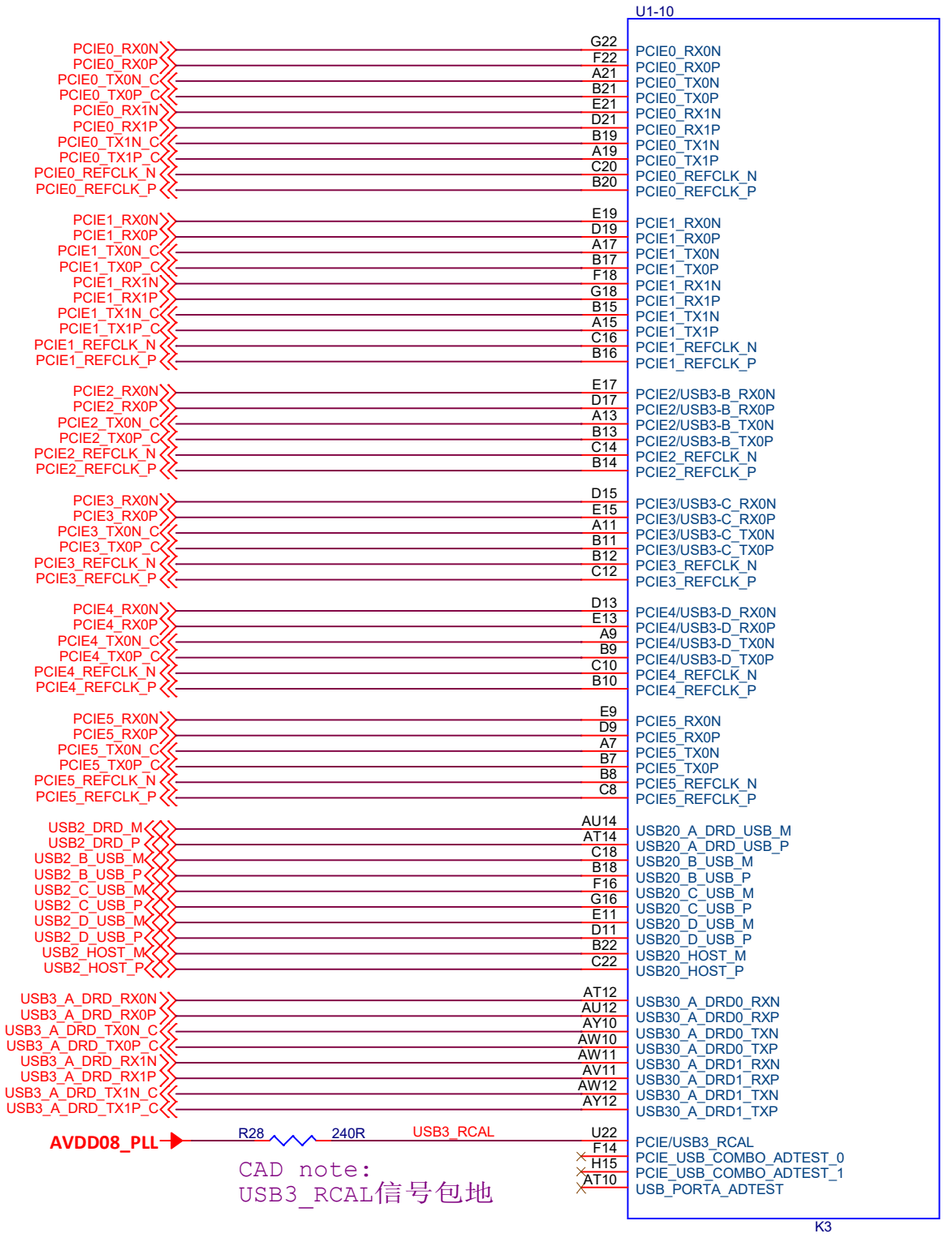
SPACEMIT 进迭时空

Document Number	<Doc>	
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 8 of 29	

K3-UFS&PCIE&USB



note:
PCIE TX和USB3 TX需要串220nF隔直电容；
所有隔直电容靠近Connect放置



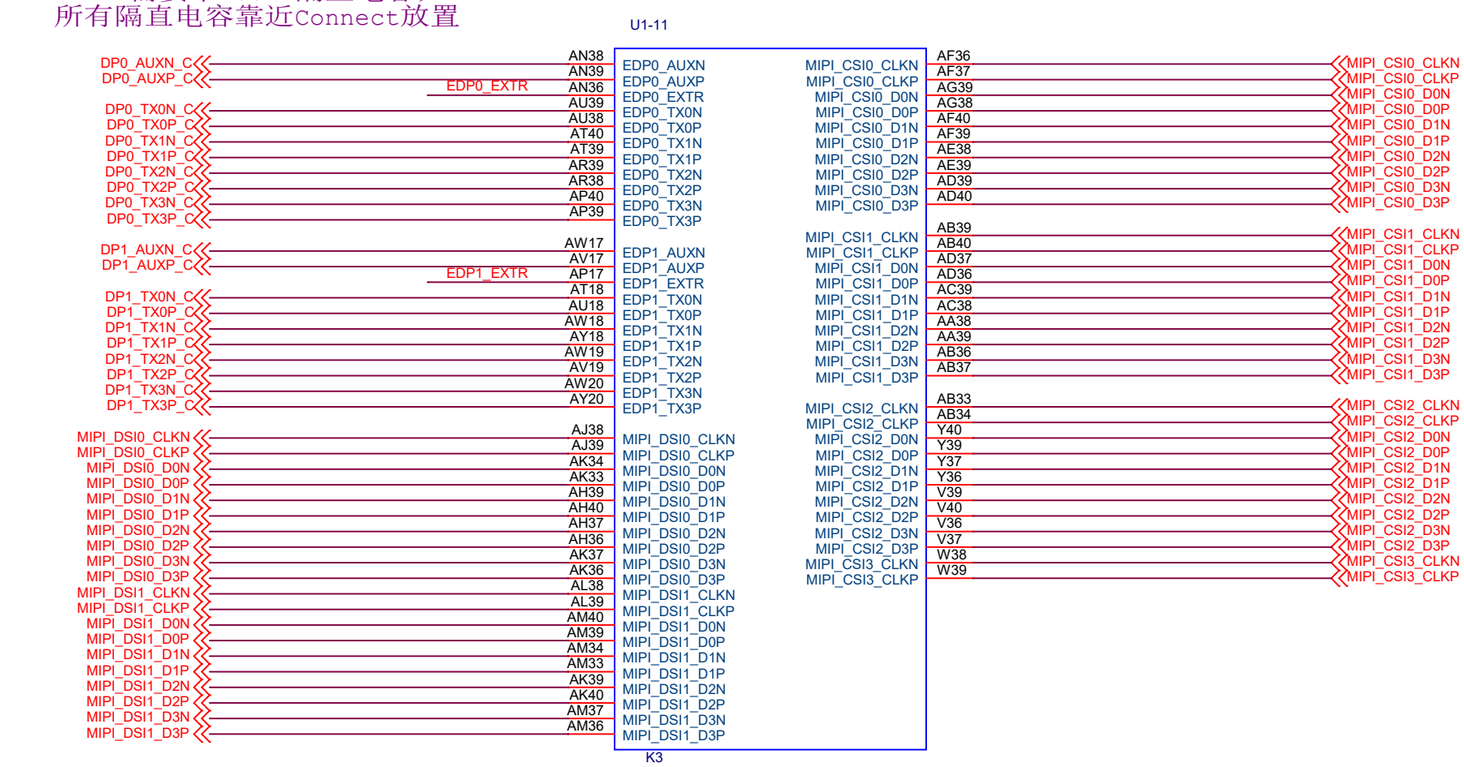
CAD note:
USB3_RCAL信号包地

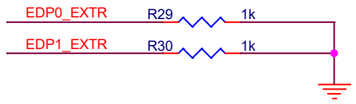
SPACEMIT 进迭时空

Document Number <Doc>		
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 9 of 29	

K3-DP&MPI

note:
DP TX需要串100nF隔直电容;
所有隔直电容靠近Connect放置

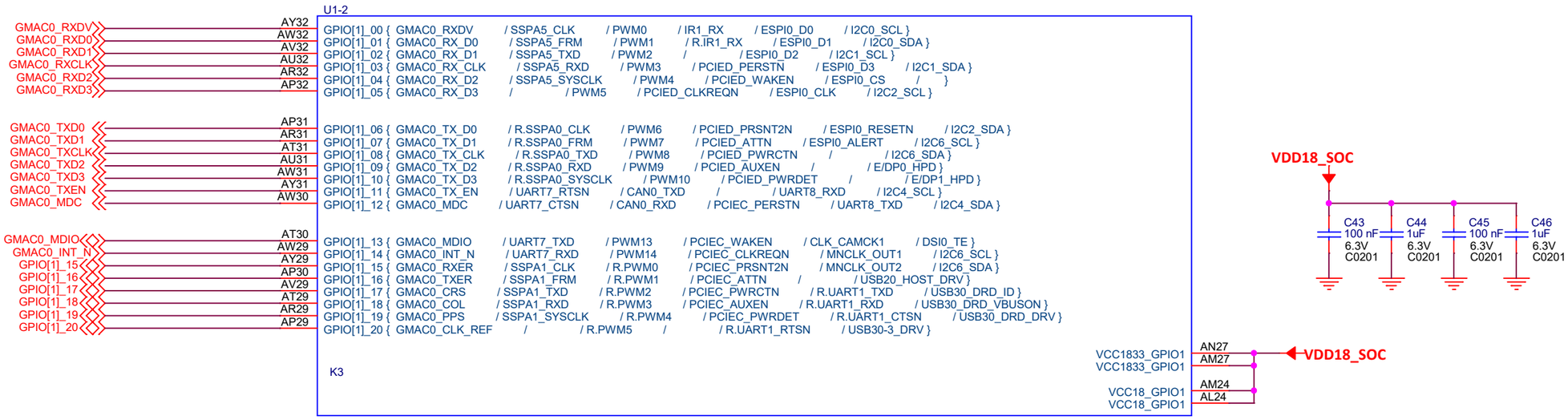


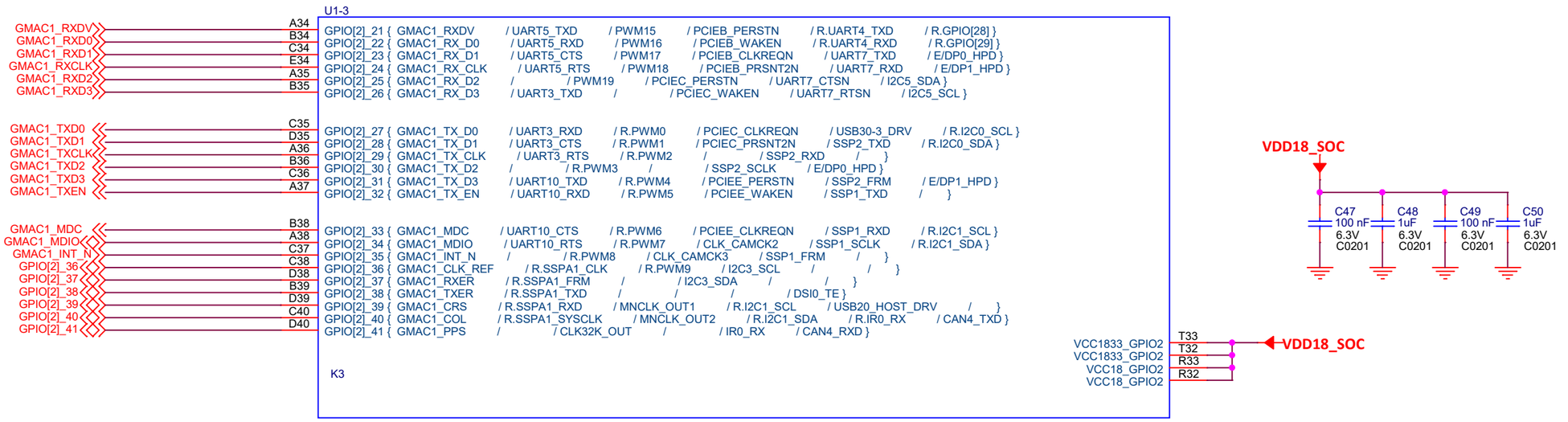


SPACEMIT 进迭时空

Document Number <Doc>		
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 10 of 29	

K3-GPIO1&2

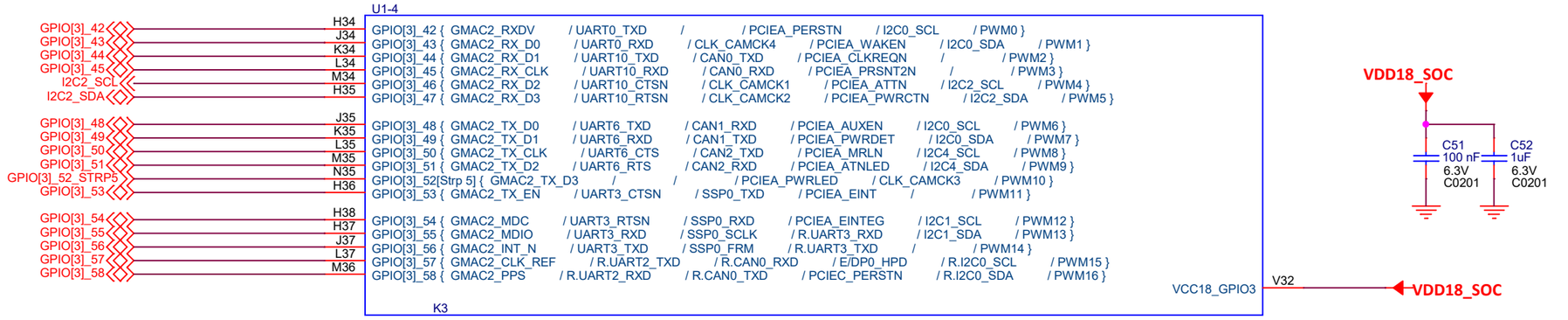


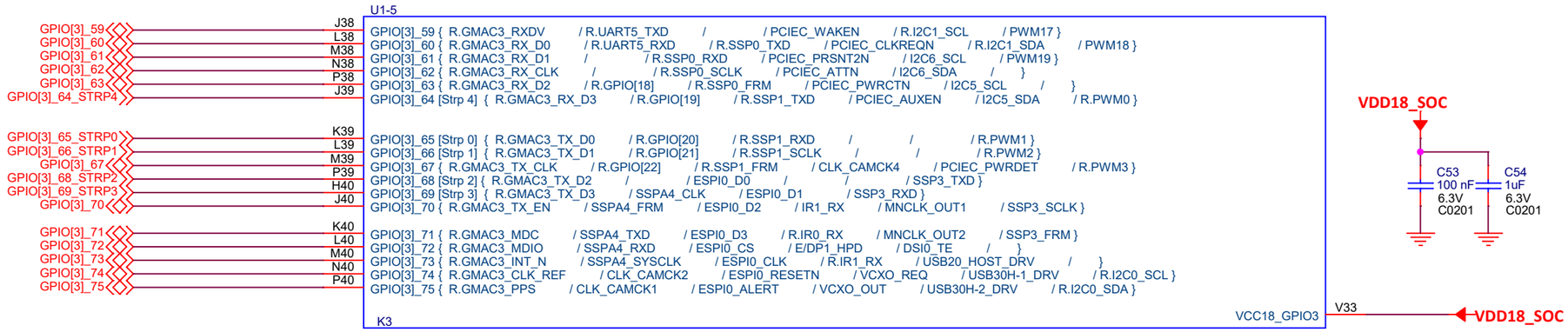


SPACEMIT 进迭时空

Document Number <Doc>		
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 11 of 29	

K3-GPIO3





Document Number	<Doc>	
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 12 of 29	

K3-GPIO4&5

U1-6

GPIO[4]_76 AR33
GPIO[4]_77 AT33
GPIO[4]_78 AP35
GPIO[4]_79 AP34
GPIO[4]_80 AR34

GPIO[4]_81 AT34
GPIO[4]_82 AV34
GPIO[4]_83 AW34
GPIO[4]_84 AY34

GPIO[4]_85 AY33
MMC1_SD AT35
GPIO[4]_87 AU35
GPIO[4]_88 AV35
GPIO[4]_89 AW35

GPIO[4]_90 AT36
GPIO[4]_91 AW36
GPIO[4]_92 AY36
GPIO[4]_93 AW37
GPIO[4]_94 AY37
GPIO[4]_95 AW38

GPIO[4]_96 AV39
DP0_HPD AW39
DP1_HPD AV40

GPIO[4]_76 { R.SSPA0_CLK / SSPA2_CLK / UART8_TXD / CAN0_TXD / PCIEE_PERSTN / I2C0_SCL }
GPIO[4]_77 { R.SSPA0_FRM / SSPA2_FRM / UART8_RXD / CAN0_RXD / PCIEE_WAKEN / I2C0_SDA }
GPIO[4]_78 { R.SSPA0_TXD / SSPA2_TXD / UART8_CTS / / PCIEE_CLKREQN / I2C1_SCL }
GPIO[4]_79 { R.SSPA0_RXD / SSPA2_RXD / UART8_RTS / / PCIEA_PERSTN / I2C1_SDA }
GPIO[4]_80 { R.SSPA0_SYSCLK / SSPA2_SYSCLK / R.UART4_TXD / CAN3_RXD / PCIEA_WAKEN / I2C2_SCL }

GPIO[4]_81 { SSP0_TXD / SSPA0_CLK / R.UART4_RXD / CAN3_TXD / PCIEA_CLKREQN / I2C2_SDA }
GPIO[4]_82 { SSP0_RXD / SSPA0_FRM / UART9_CTSN / UART5_RXD / PCIEA_PRSNT2N / I2C3_SCL }
GPIO[4]_83 { SSP0_SCLK / SSPA0_TXD / UART9_RTSN / UART5_TXD / PCIEA_ATTN / I2C3_SDA }
GPIO[4]_84 { SSP0_FRM / SSPA0_RXD / UART9_TXD / USB30-1_DRV / PCIEA_PWRCTN / DSI0_TE }

GPIO[4]_85 { CLK_CAMCK3 / SSPA0_SYSCLK / UART9_RXD / USB30-2_DRV / PCIEA_AUXEN / }
GPIO[4]_86 { R.SSP0_TXD / R.ESPI0_D0 / UART4_TXD / CAN2_TXD / PCIEA_PWRDET / USB30-0_DIR }
GPIO[4]_87 { R.SSP0_RXD / R.ESPI0_D1 / UART4_RXD / CAN2_RXD / PCIEA_MRLN / PCIEB_PRSNT2N }
GPIO[4]_88 { R.SSP0_SCLK / R.ESPI0_D2 / R.UART3_TXD / PCIEB_PERSTN / PCIEA_ATNLED / CAN1_RXD }
GPIO[4]_89 { R.SSP0_FRM / R.ESPI0_D3 / R.UART3_RXD / PCIEB_WAKEN / PCIEA_PWRLED / CAN1_TXD }

GPIO[4]_90 { DSI0_TE / R.ESPI0_CS / UART4_CTSN / PCIEB_CLKREQN / PCIEA_EINT / R.CAN0_RXD }
GPIO[4]_91 { R.GPIO[23] / R.ESPI0_CLK / UART4_RTSN / ESPI0_D0 / PCIEA_EINTEG / R.CAN0_TXD }
GPIO[4]_92 { R.GPIO[24] / R.ESPI0_RESETN / / ESPI0_D1 / R.PWM5 / DSI0_TE }
GPIO[4]_93 { R.GPIO[25] / R.ESPI0_ALERT / UART0_TXD / ESPI0_D2 / I2C5_SCL / R.PWM4 }
GPIO[4]_94 { R.GPIO[26] / / UART0_RXD / ESPI0_D3 / I2C5_SDA / R.PWM6 }
GPIO[4]_95 { R.GPIO[27] / UART1_TXD<SECURE DOMAIN> / USB30_DRD_ID / ESPI0_CS / / PWM1 }

GPIO[4]_96 { / UART1_RXD<SECURE DOMAIN> / USB30_DRD_VBUSON / ESPI0_CLK / / PWM2 }
GPIO[4]_97 { UART2_TXD / UART1_CTS<SECURE DOMAIN> / USB30_DRD_DRV / ESPI0_RESETN / E/DP0_HPD / PWM3 }
GPIO[4]_98 { UART2_RXD / UART1_RTS<SECURE DOMAIN> / CLK32K_OUT / ESPI0_ALERT / E/DP1_HPD / }

VCC1833_GPIO4 AN26
VCC1833_GPIO4 AM26
VCC18_GPIO4 AL26
VCC18_GPIO4 AL25

VDD18_SOC
VDD18_SOC
C55 100 nF 6.3V C0201
C56 1uF 6.3V C0201
C57 100 nF 6.3V C0201
C58 1uF 6.3V C0201

K3

U1-7

GPIO[5]_99 AR28
GPIO[5]_100 AT28
GPIO[5]_101 AU28
GPIO[5]_102 AV28
GPIO[5]_103 AY28

GPIO[5]_104 AW27
GPIO[5]_105 AR27
GPIO[5]_106 AP27
GPIO[5]_107 AY27

GPIO[5]_108 AP26
GPIO[5]_109 AR26
GPIO[5]_110 AT26
GPIO[5]_111 AU26
GPIO[5]_112 AW26
GPIO[5]_113 AY26
GPIO[5]_114 AP25
GPIO[5]_115 AT25

GPIO[5]_116 AU25
GPIO[5]_117 AV25
GPIO[5]_118 AW25
GPIO[5]_119 AP24
UART1_RXD AR24
UART1_TXD AT24

GPIO[5]_122 AW24
GPIO[5]_123 AY24
GPIO[5]_124 AT23
GPIO[5]_125 AU23
GPIO[5]_126 AV23
GPIO[5]_127 AY23

GPIO[5]_99 { SSP3_TXD / SSPA3_CLK / UART4_TXD / R.CAN2_TXD / / CLK_CAMCK4 }
GPIO[5]_100 { SSP3_RXD / SSPA3_FRM / UART4_RXD / R.CAN2_RXD / PCIED_PRSNT2N / CLK32K_OUT }
GPIO[5]_101 { SSP3_SCLK / SSPA3_TXD / UART4_CTS / CAN4_RXD / PCIED_ATTN / MNCLK_OUT1 }
GPIO[5]_102 { SSP3_FRM / SSPA3_RXD / UART4_RTS / CAN4_TXD / PCIED_PWRCTN / I2C1_SCL }
GPIO[5]_103 { / SSPA3_SYSCLK / USB20_HOST_DRV / CAN3_TXD / PCIED_AUXEN / I2C1_SDA }

GPIO[5]_104 { SSP0_TXD / SSP2_TXD / USB30H-1_DRV / CAN3_RXD / PCIED_PWRDET / }
GPIO[5]_105 { SSP0_RXD / SSP2_RXD / R.I2C1_SCL / I2C3_SCL / PCIED_PERSTN / PWM17 }
GPIO[5]_106 { SSP0_SCLK / SSP2_SCLK / R.I2C1_SDA / I2C3_SDA / PCIED_WAKEN / PWM18 }
GPIO[5]_107 { SSP0_FRM / SSP2_FRM / R.CAN4_TXD / USB30-0_DIR / PCIED_CLKREQN / PWM19 }

GPIO[5]_108 { R.SSP1_TXD / USB20_HOST_DRV / R.CAN4_RXD / IR0_RX / PCIEA_PERSTN / }
GPIO[5]_109 { R.SSP1_RXD / / R.UART0_TXD / CAN1_TXD / PCIEA_WAKEN / R.PWM6 }
GPIO[5]_110 { / / R.UART0_RXD / CAN1_RXD / PCIEA_CLKREQN / R.PWM7 }
GPIO[5]_111 { SSP1_TXD / SSPA0_CLK / UCIE_DESCL / I2C4_SCL / USB30-0_INT / R.PWM8 }
GPIO[5]_112 { SSP1_RXD / SSPA0_FRM / UCIE_DESDA / I2C4_SDA / USB30-3_DRV / R.PWM9 }
GPIO[5]_113 { SSP1_SCLK / SSPA0_TXD / R.GPIO[30] / / PCIEB_PERSTN / }
GPIO[5]_114 { SSP1_FRM / SSPA0_RXD / R.GPIO[31] / / PCIEB_WAKEN / }
GPIO[5]_115 { / SSPA0_SYSCLK / R.GPIO[32] / I2C0_SCL / PCIEB_CLKREQN / R.I2C0_SCL }

GPIO[5]_116 { R.SSP1_SCLK / USB30_DRD_ID / R.GPIO[33] / I2C0_SDA / PCIEB_PRSNT2N / R.I2C0_SDA }
GPIO[5]_117 { R.SSP1_FRM / USB30_DRD_VBUSON / R.GPIO[34] / / PCIEB_ATTN / }
GPIO[5]_118 { UART1_RTSN<SECURE DOMAIN> / USB30_DRD_DRV / R.GPIO[35] / / PCIEB_PWRCTN / }
GPIO[5]_119 { UART1_CTSN<SECURE DOMAIN> / USB30-0_INT / / / PCIEB_AUXEN / }
GPIO[5]_120 { UART1_RXD<SECURE DOMAIN> / I2C2_SCL / R.CAN3_TXD / CAN4_TXD / PCIEB_PWRDET / }
GPIO[5]_121 { UART1_TXD<SECURE DOMAIN> / I2C2_SDA / R.CAN3_RXD / CAN4_RXD / PCIEB_MRLN / }

GPIO[5]_122 { MMC2_DAT[3] / SSPA1_CLK / UART6_TXD / R.UART0_TXD / PCIEB_ATNLED / }
GPIO[5]_123 { MMC2_DAT[2] / SSPA1_FRM / UART6_RXD / R.UART0_RXD / PCIEB_PWRLED / }
GPIO[5]_124 { MMC2_DAT[1] / SSPA1_TXD / PCIED_PERSTN / E/DP0_HPD / PCIEB_EINT / }
GPIO[5]_125 { MMC2_DAT[0] / SSPA1_RXD / PCIED_WAKEN / E/DP1_HPD / PCIEB_EINTEG / }
GPIO[5]_126 { MMC2_CMD / SSPA1_SYSCLK / PCIED_CLKREQN / I2C5_SCL / / }
GPIO[5]_127 { MMC2_CLK / / PCIED_PRSNT2N / I2C5_SDA / / USB30-2_DRV }

K3

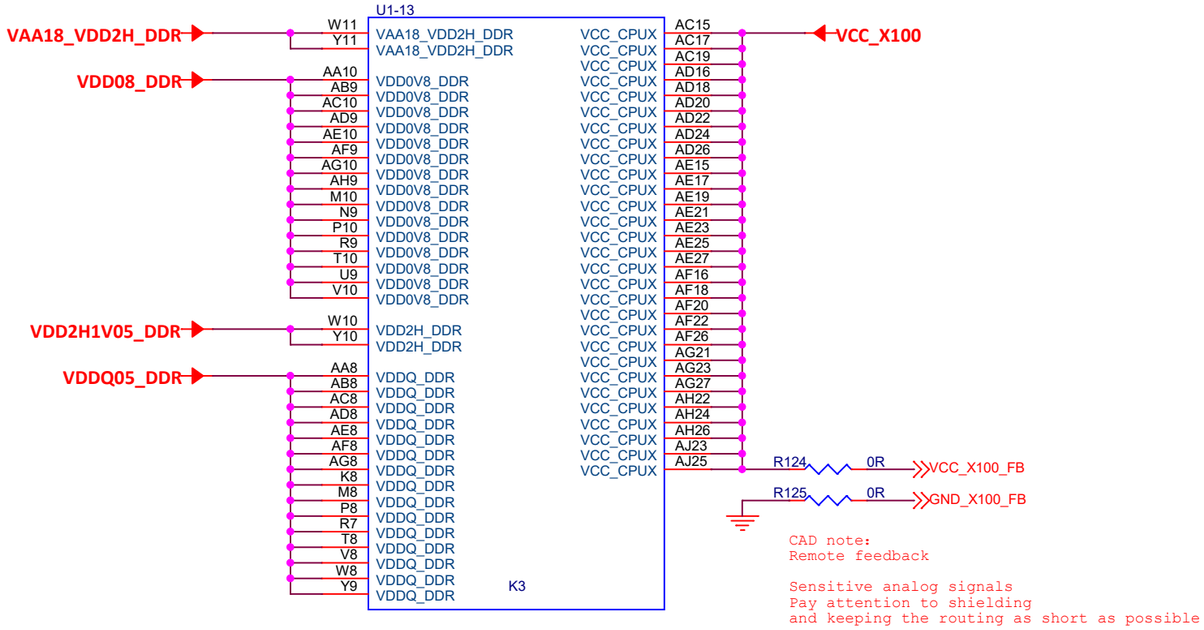
VCC1833_GPIO5 AP20
VCC1833_GPIO5 AN20
VCC18_GPIO5 AM22
VCC18_GPIO5 AL22

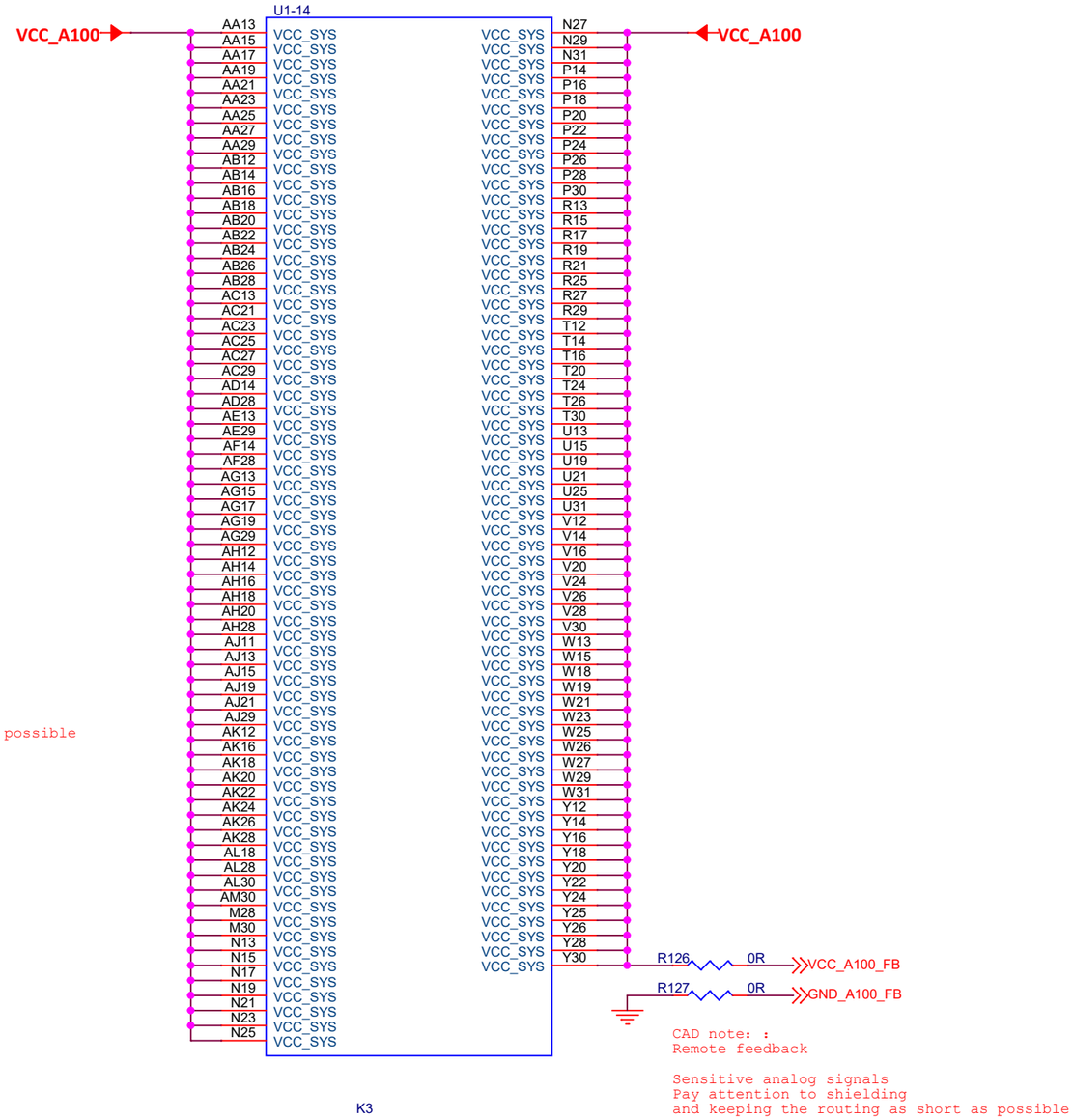
VDD18_SOC
VDD18_SOC
C59 100 nF 6.3V C0201
C60 1uF 6.3V C0201
C61 100 nF 6.3V C0201
C62 1uF 6.3V C0201

SPACEMIT 进迭时空

Document Number <Doc>		
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 13 of 29	

K3-Power(1 OF 2)

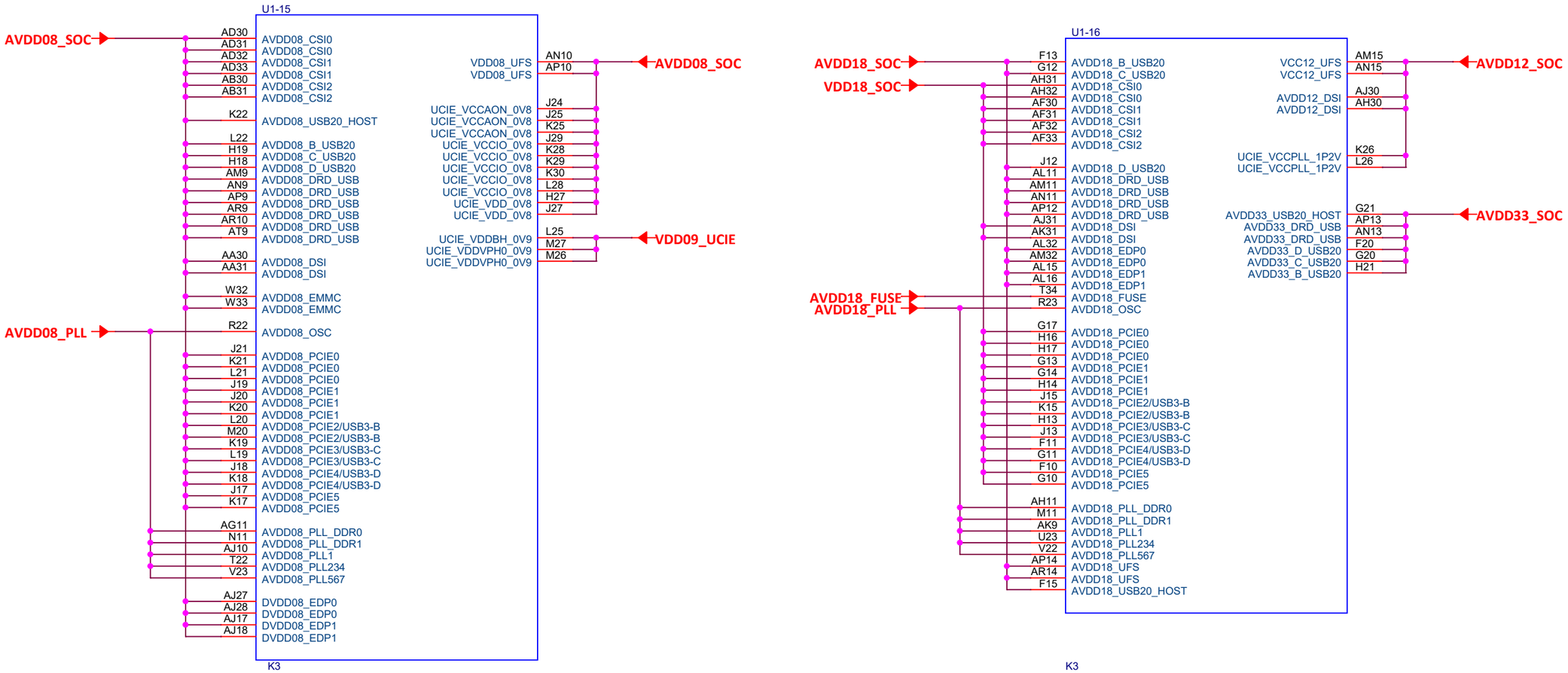




SPACEMIT 进迭时空

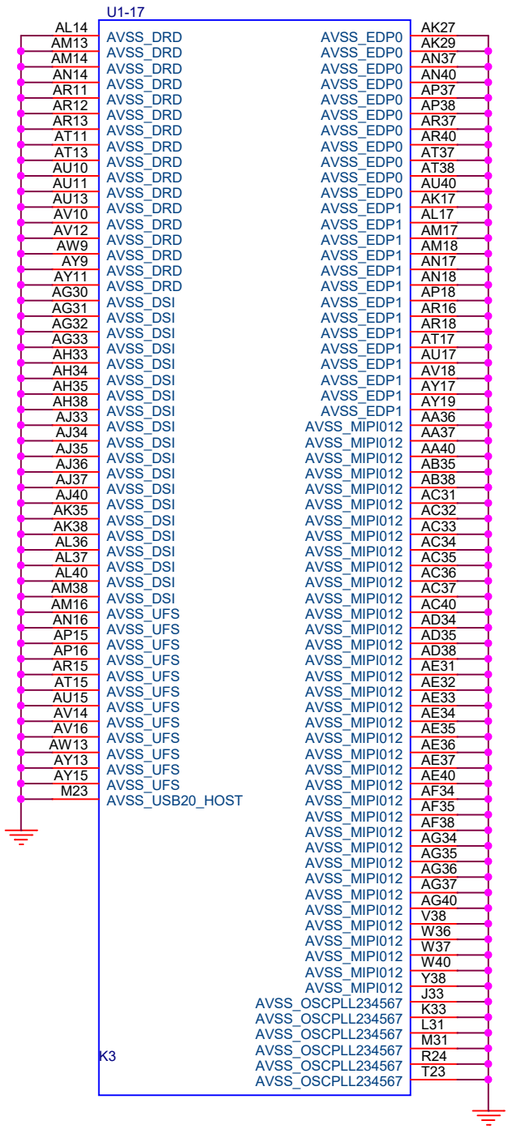
Document Number	<Doc>	
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 14 of 29	

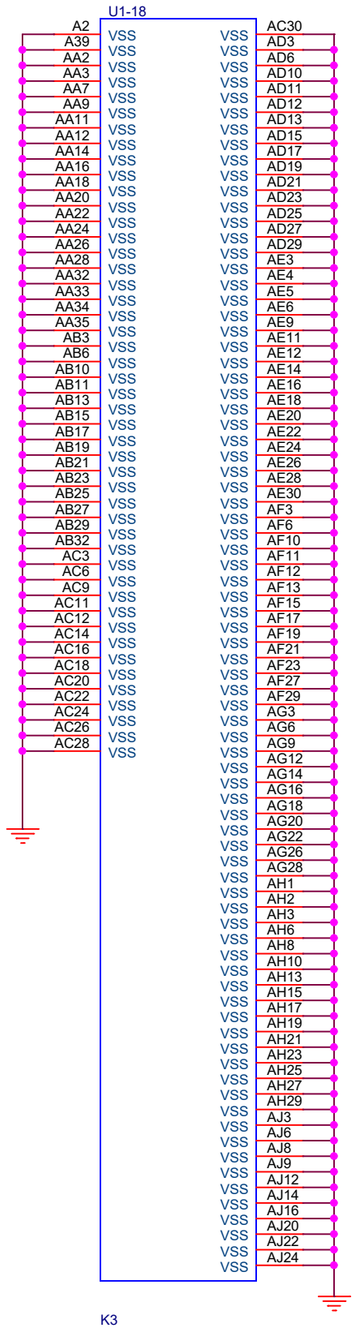
K3-Power(2 OF 2)

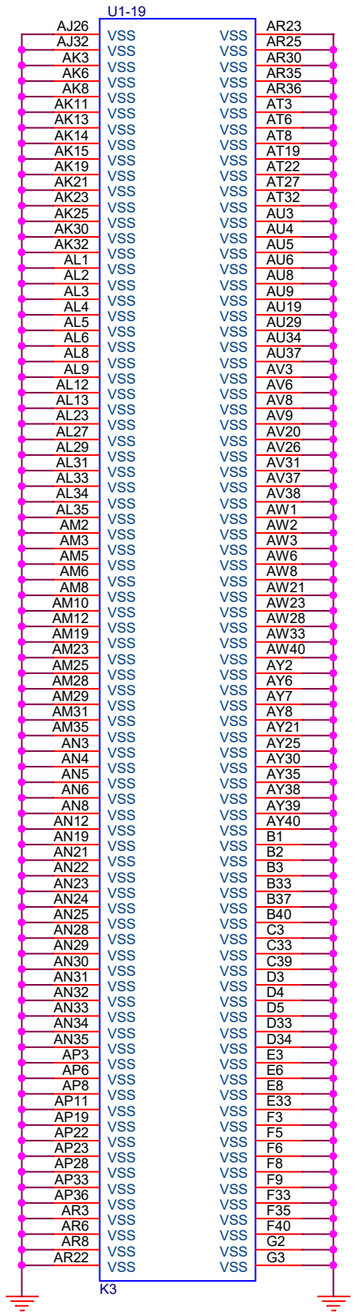


Document Number	<Doc>	
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 15 of 29	

K3-VSS(1 OF 2)







SPACEMIT 进迭时空

Document Number <Doc>		
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 16 of 29	

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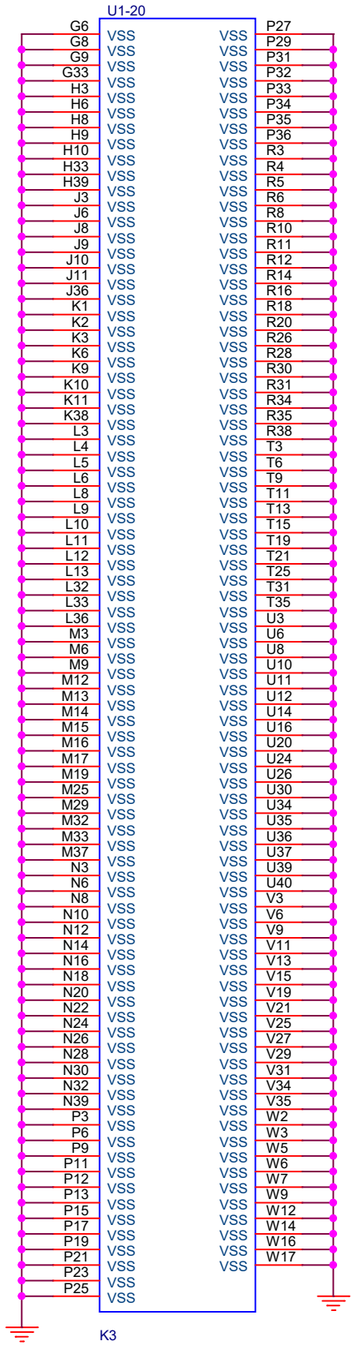

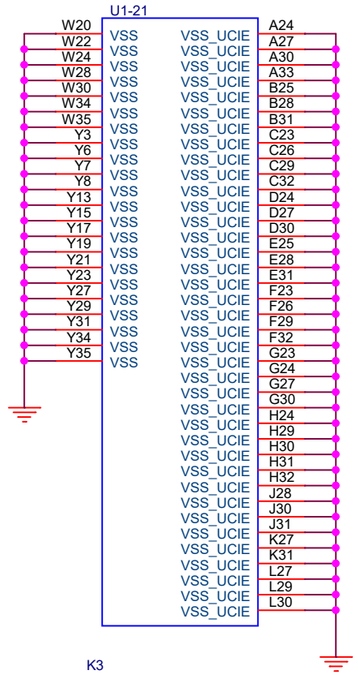

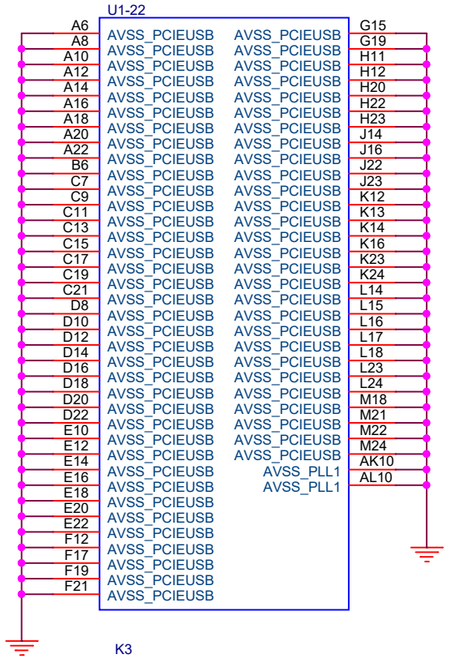

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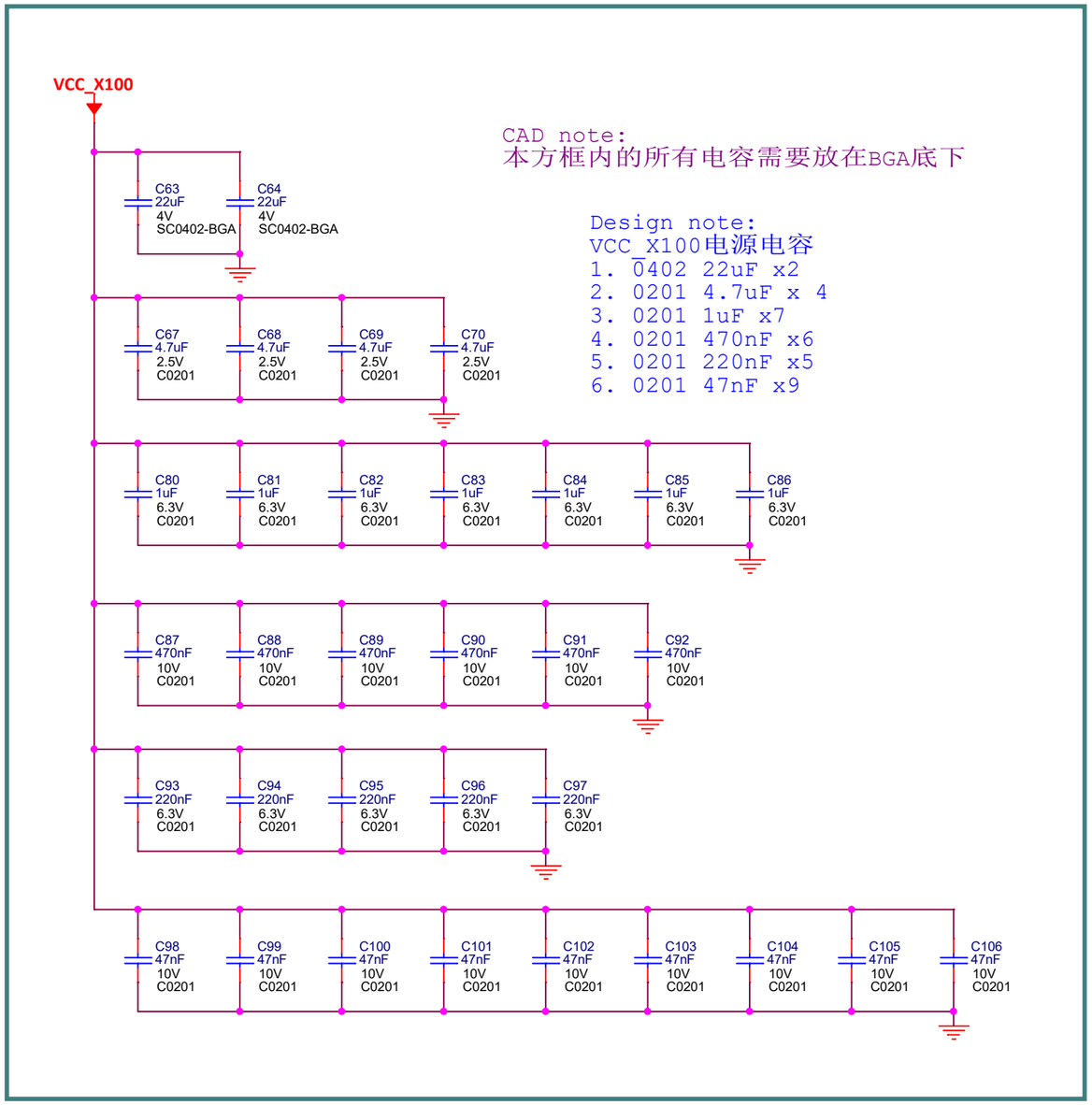
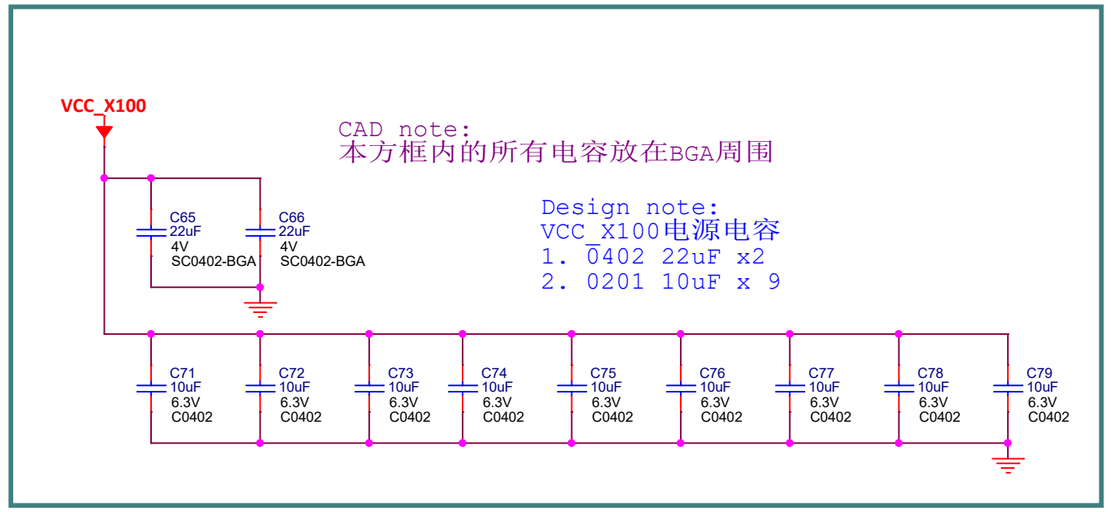
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 17 of 29	

K3-Power Decap(1 OF 3)





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Document Number <Doc>		
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 18 of 29	

K3-Power Decap(2 OF 3)

Design note:
VCC_A100电源电容
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2. 0201 4.7uF x17
3. 0201 2.2uF x17

CAD note:
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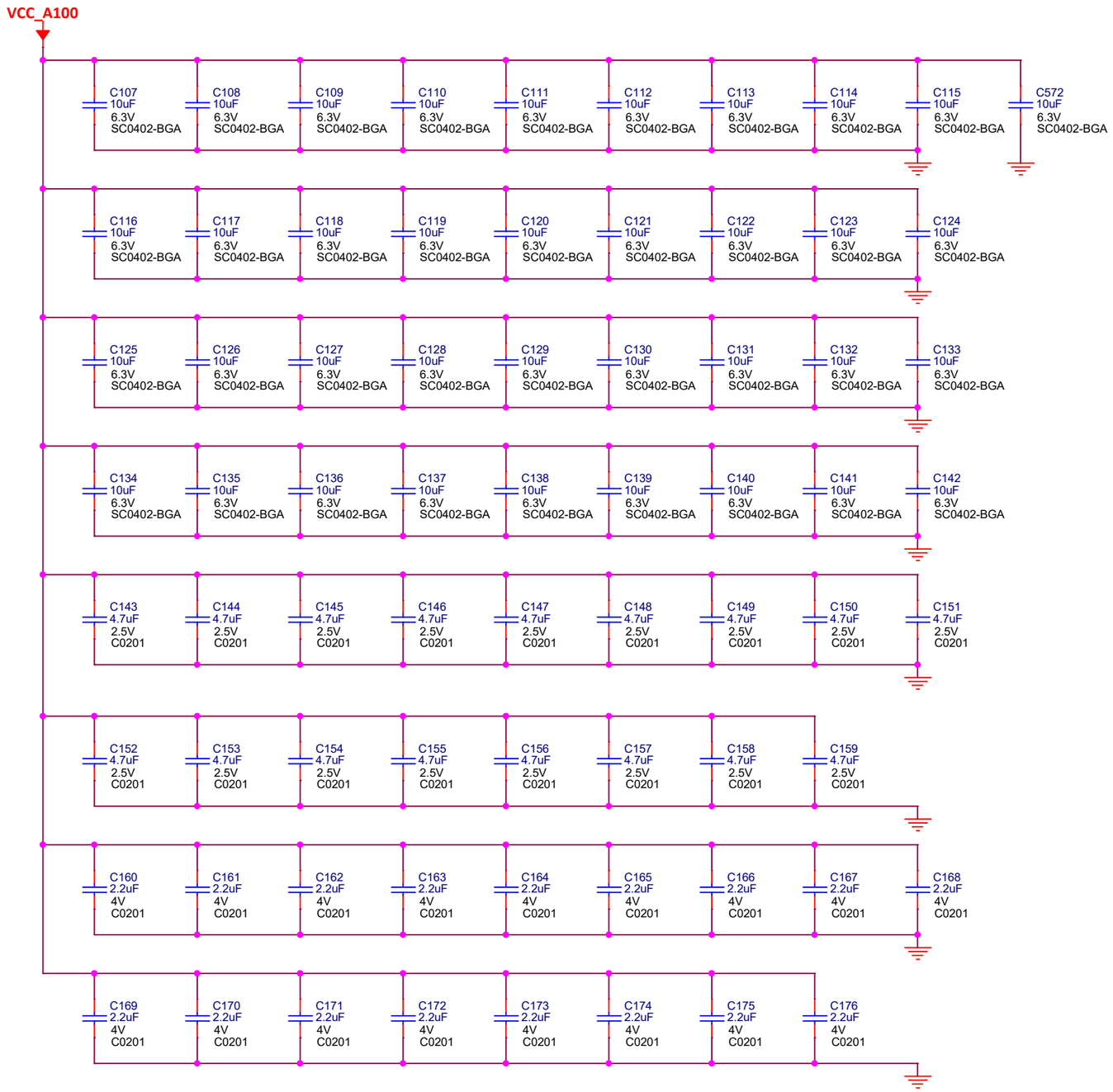

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Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 19 of 29	

K3-Power Decap(3 OF 3)

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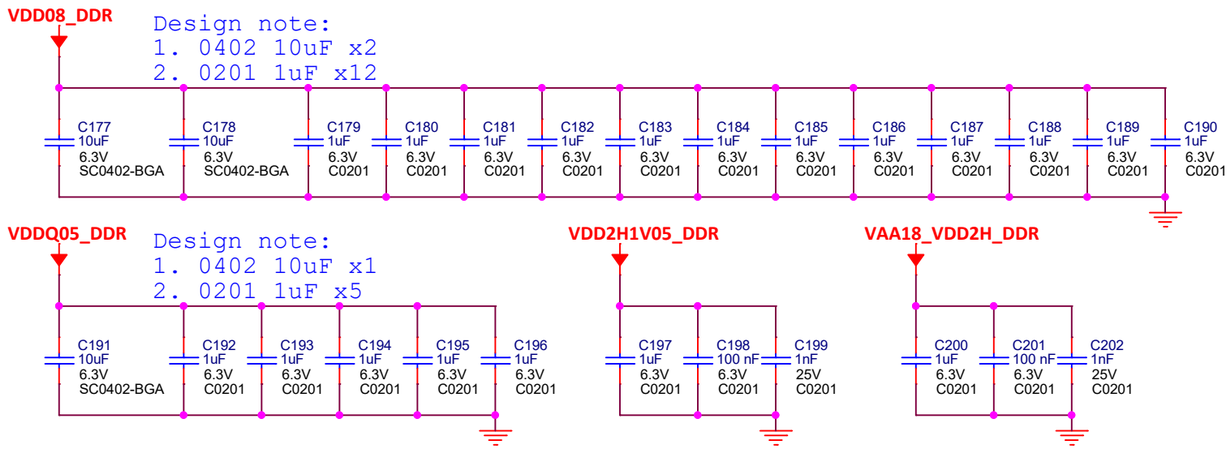

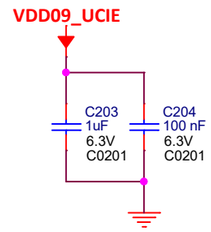

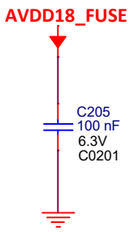

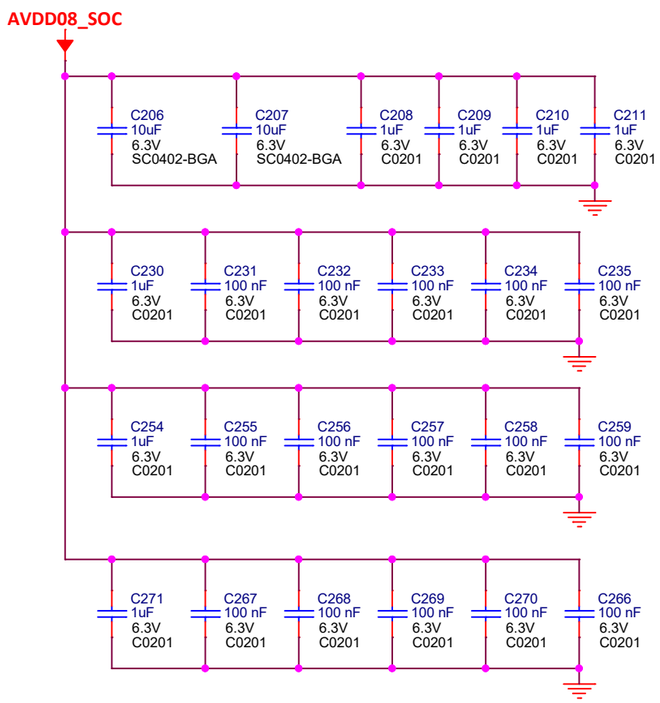

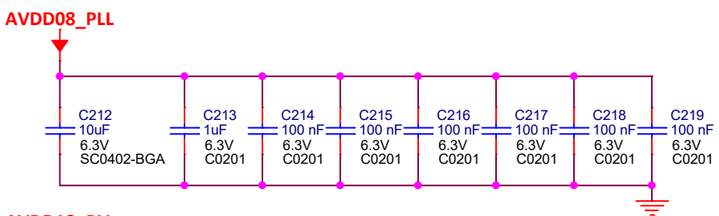

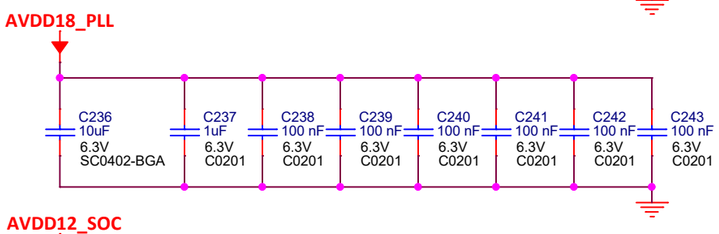

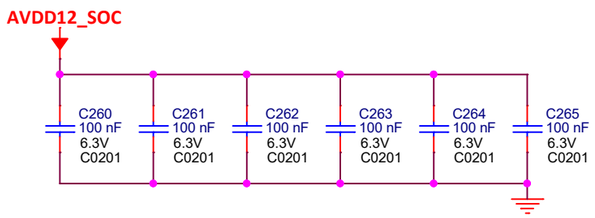

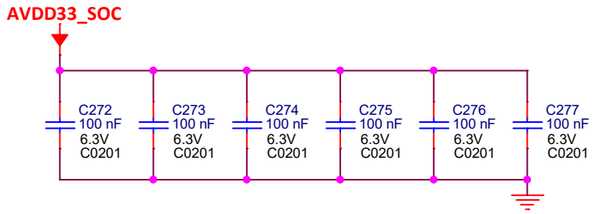

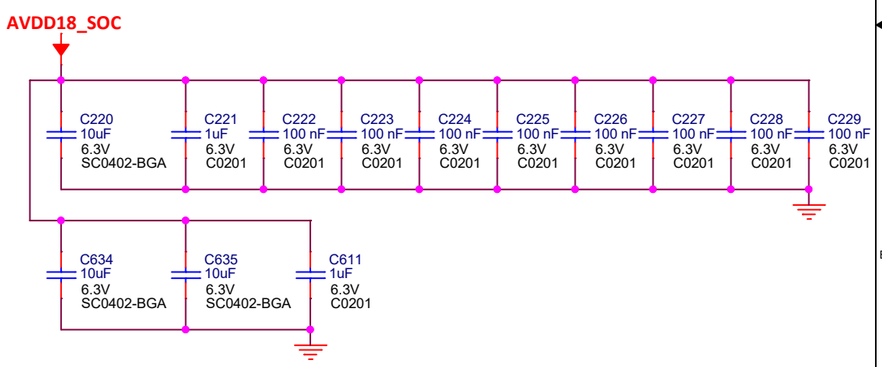

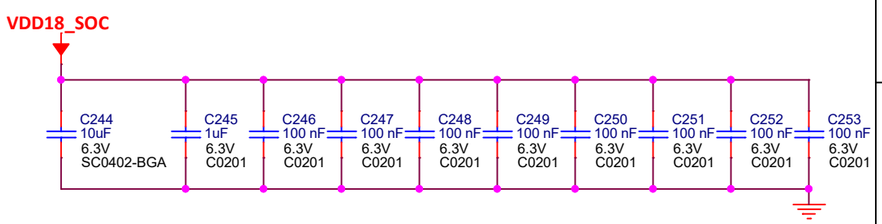

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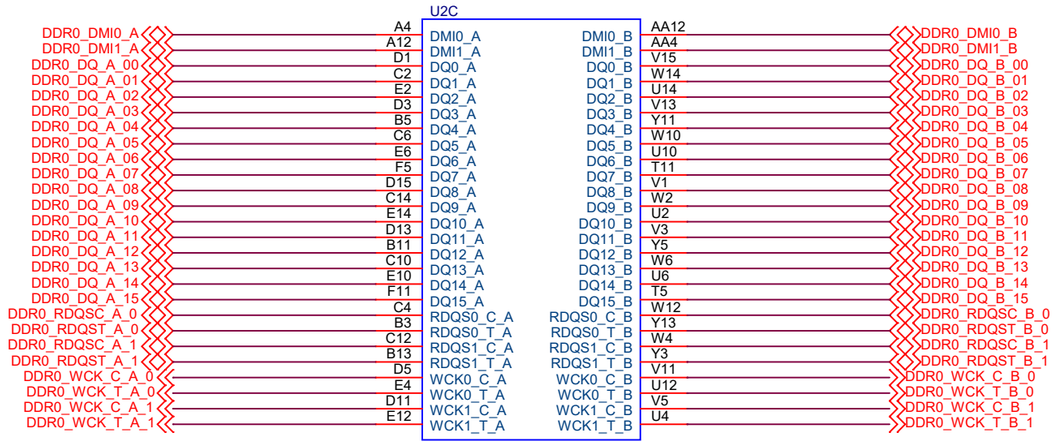
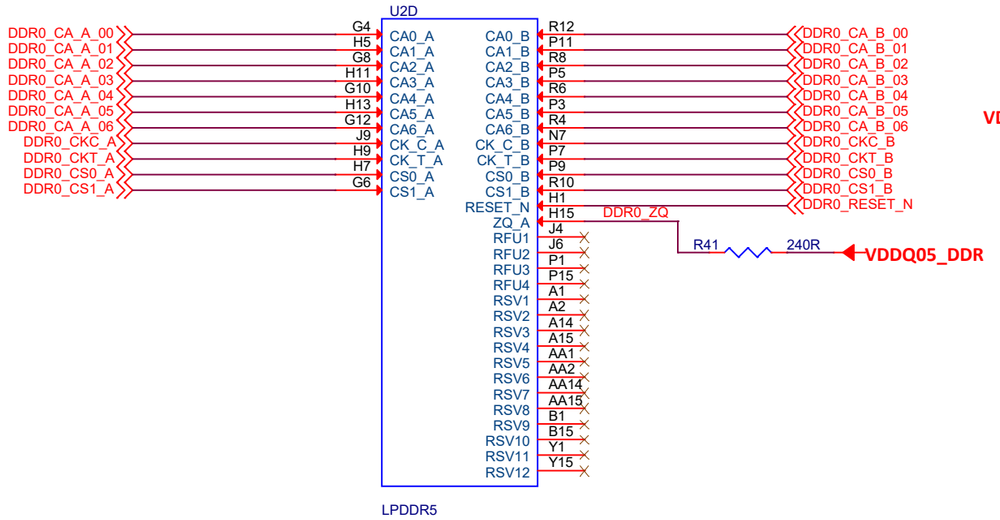
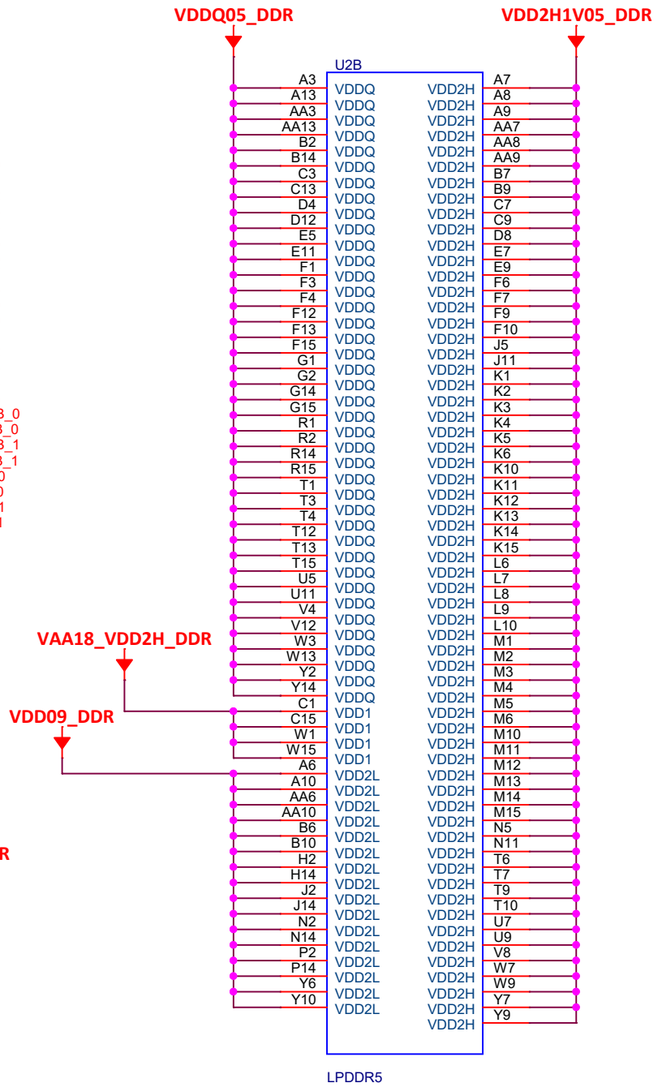
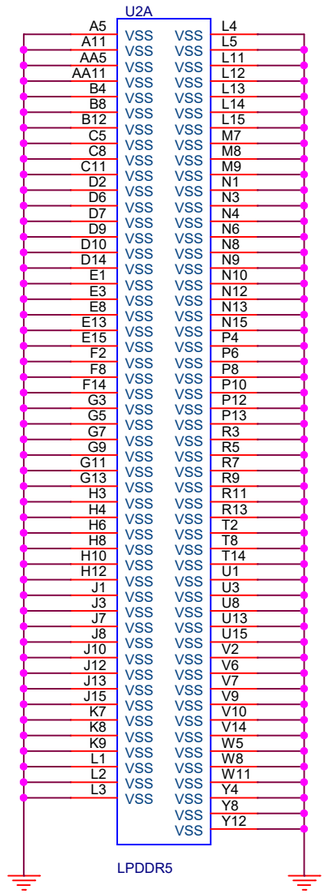
Document Number <Doc>		
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 20 of 29	

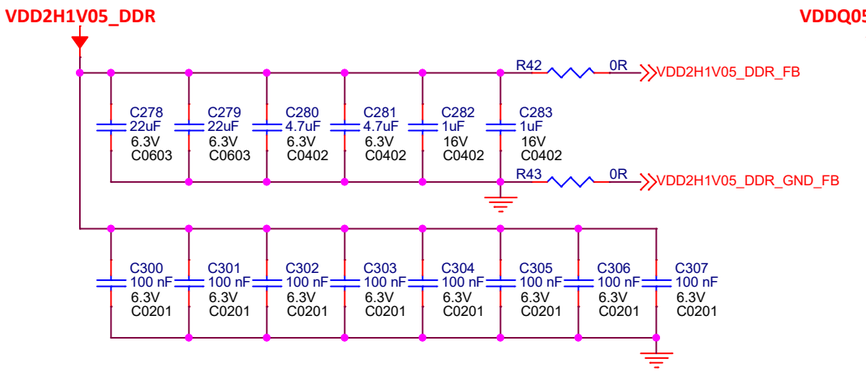
LPDDR5(1 OF 2)

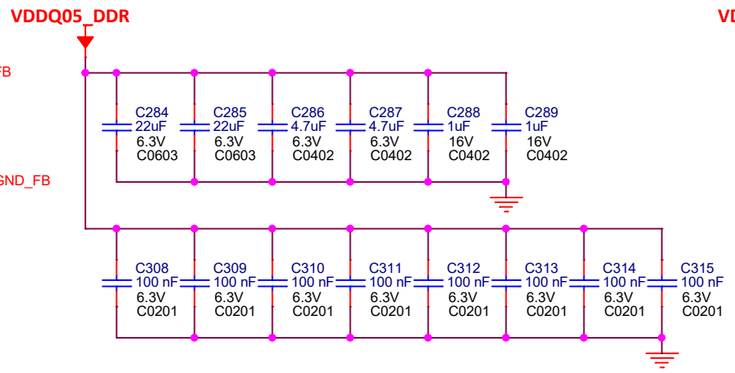


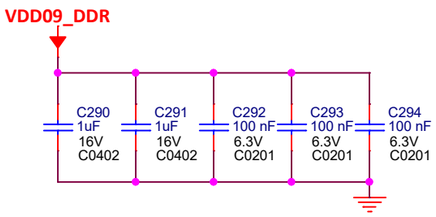


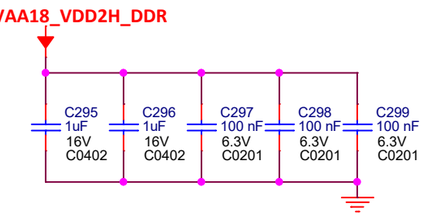












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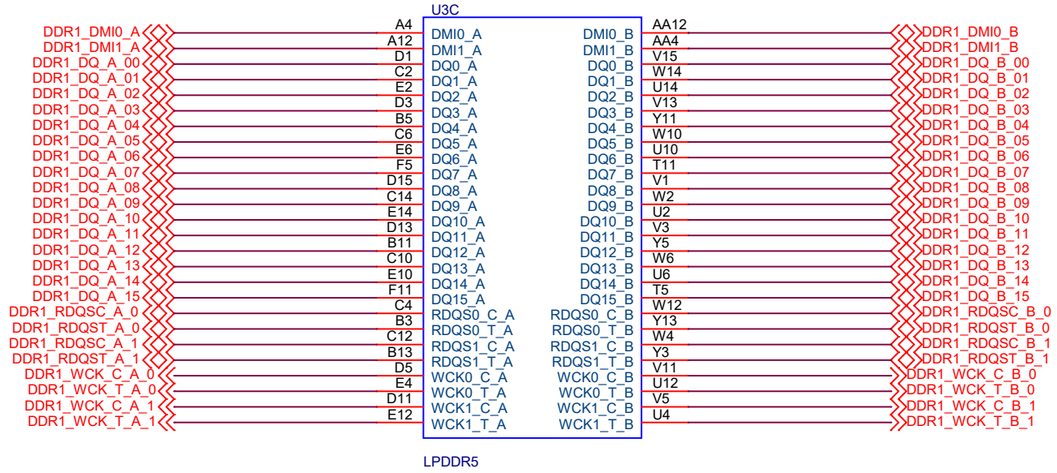
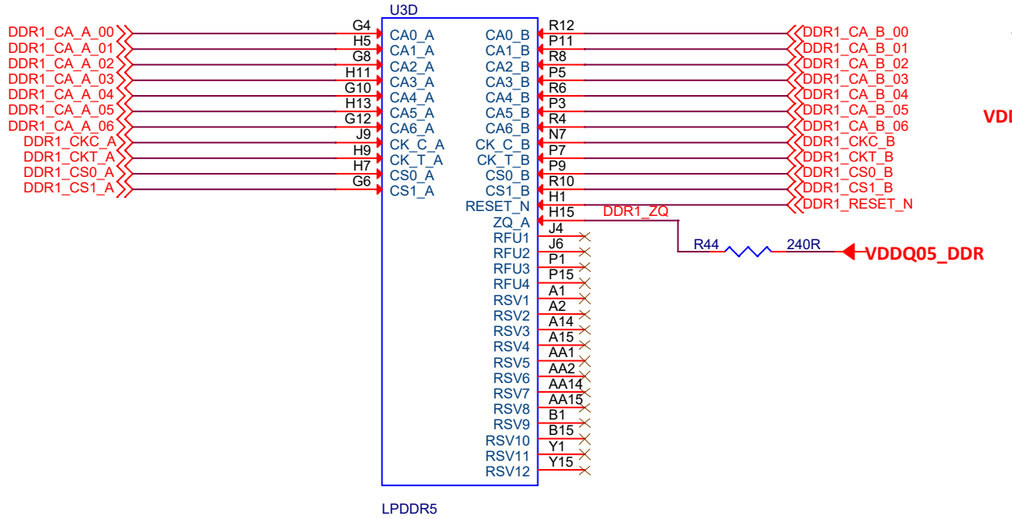
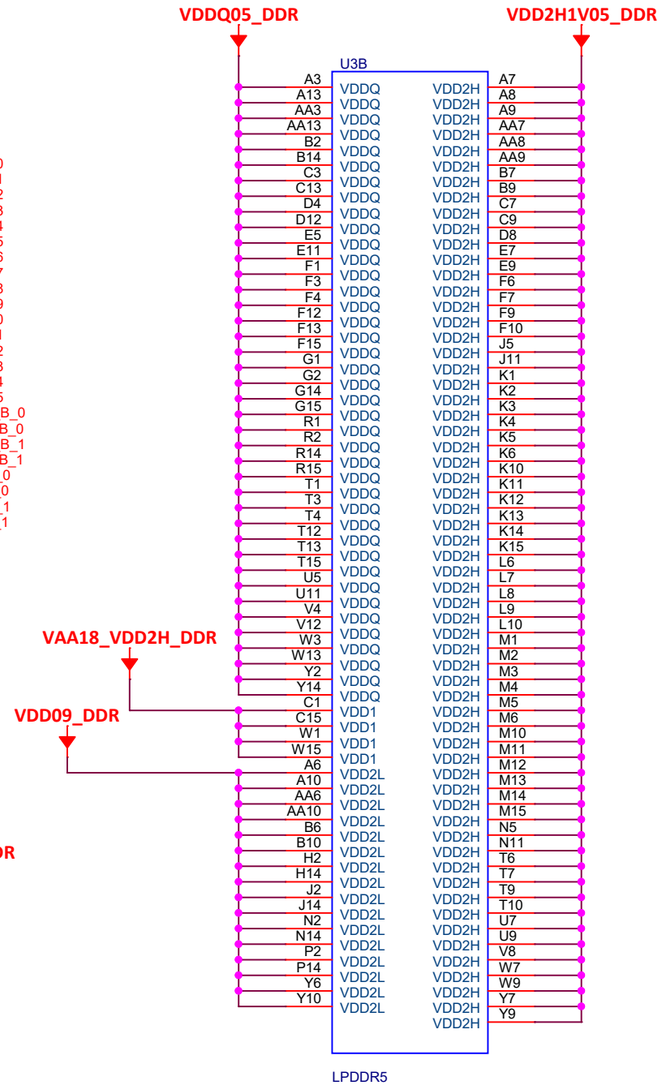
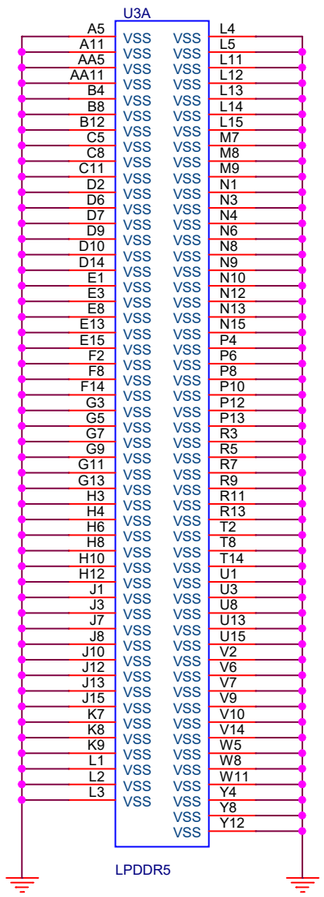
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 21 of 29	

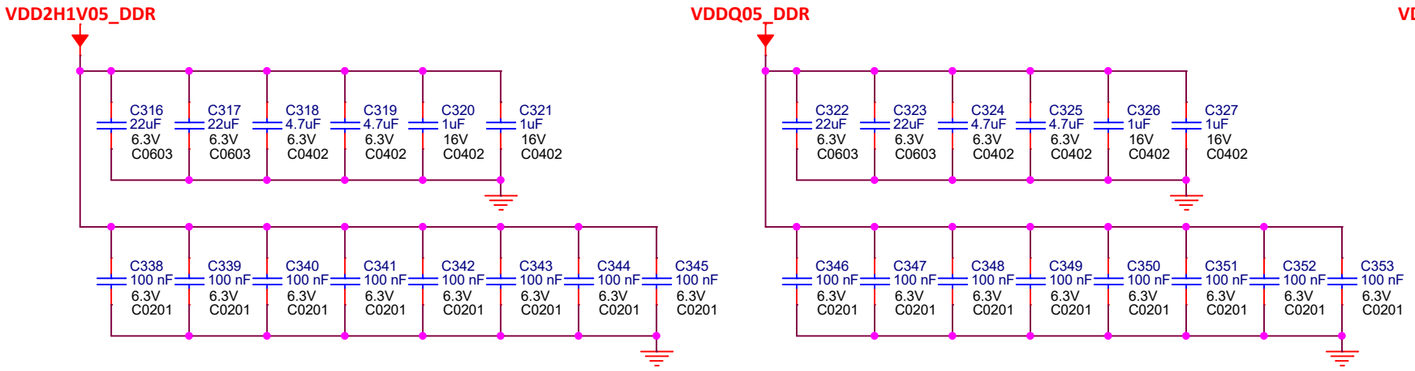
LPDDR5(2 OF 2)

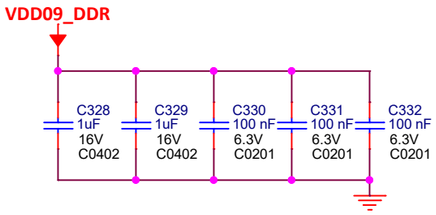


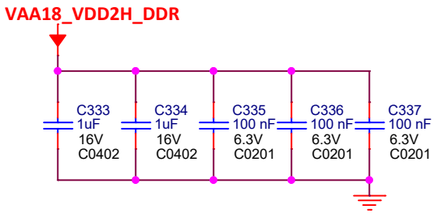












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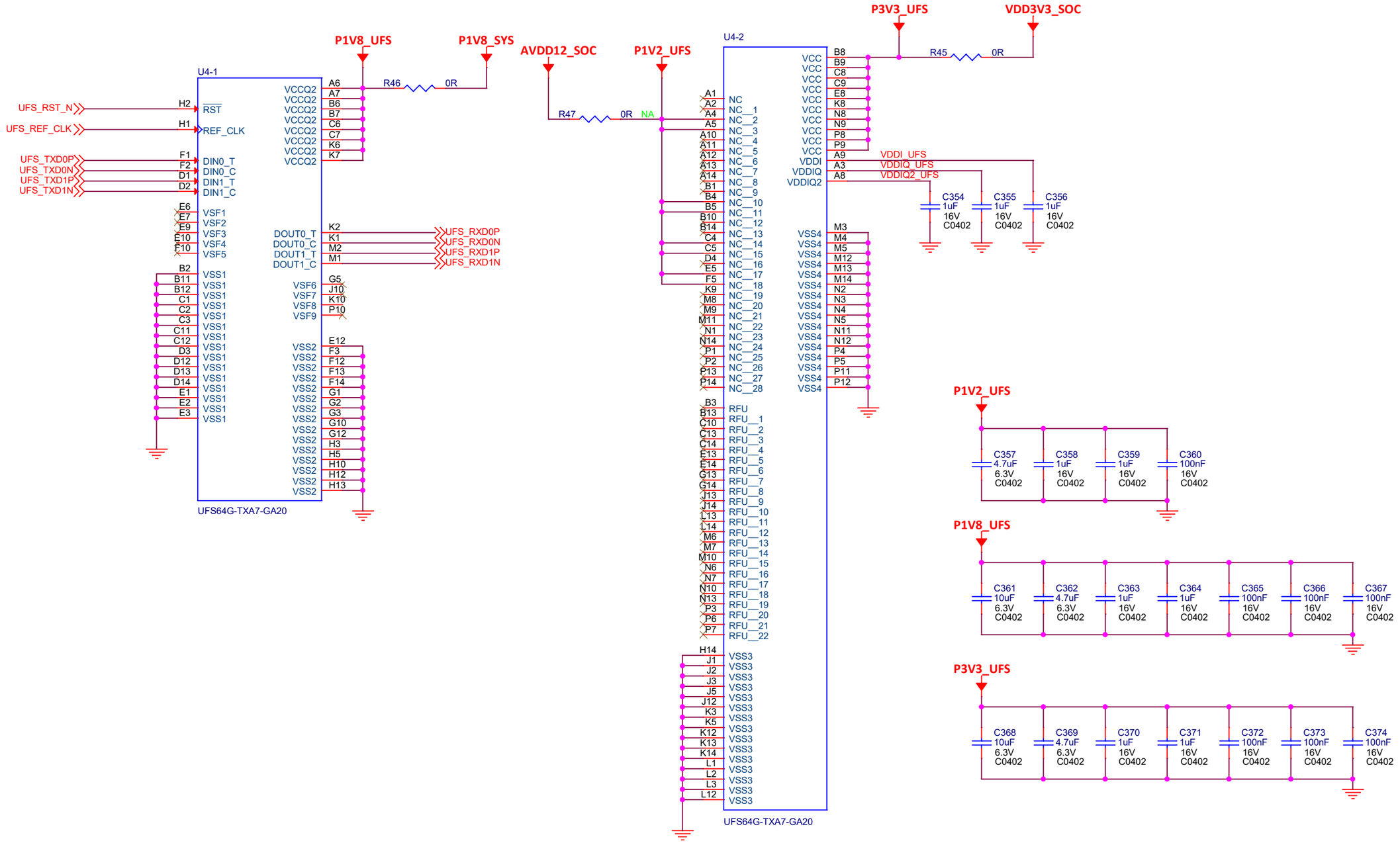
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 22 of 29	

UFS



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Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 23 of 29	

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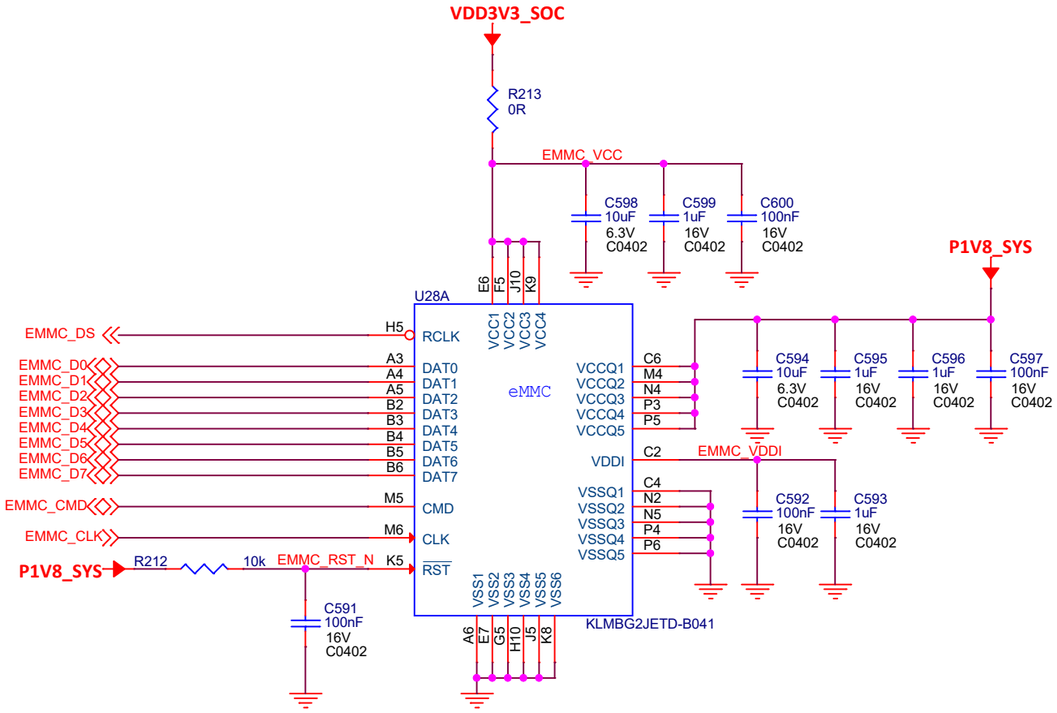

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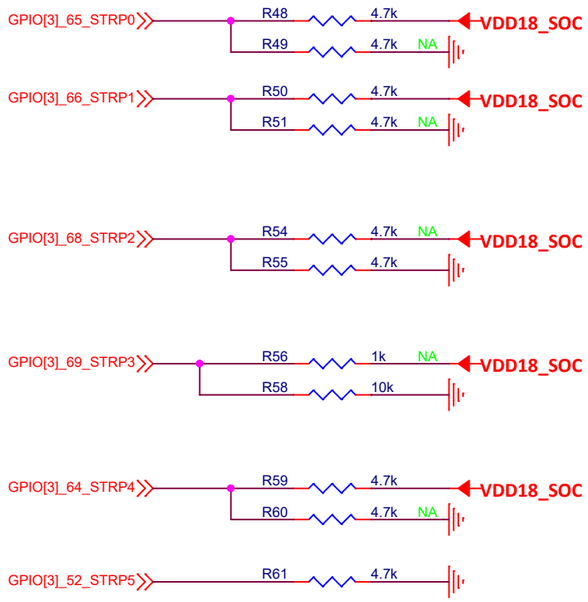
Document Number <Doc>		
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 24 of 29	

Strap&MISC



Strap Design note:

Strap1	Strap0	BOOT SEL
0	0	TF Card -> EMMC
0	1	TF Card -> SPI NOR
1	0	TF Card -> SPI NAND
1	1	TF Card -> UFS

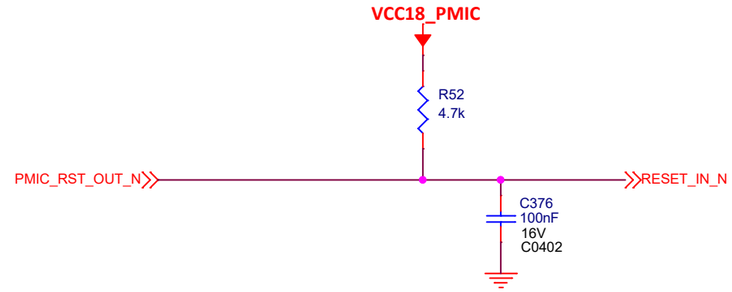
Strap2	Download SEL
0	USB
1	UART

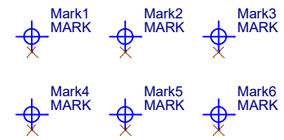
Strap3	BOOT/Download
0	启动
1	下载

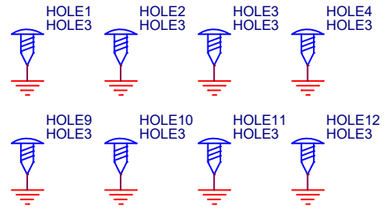
Strap4	QSPI VOL
0	3V3
1	1V8

Strap5	DDR SEL
0	LPDDR5
1	LPDDR4x

Reset K3







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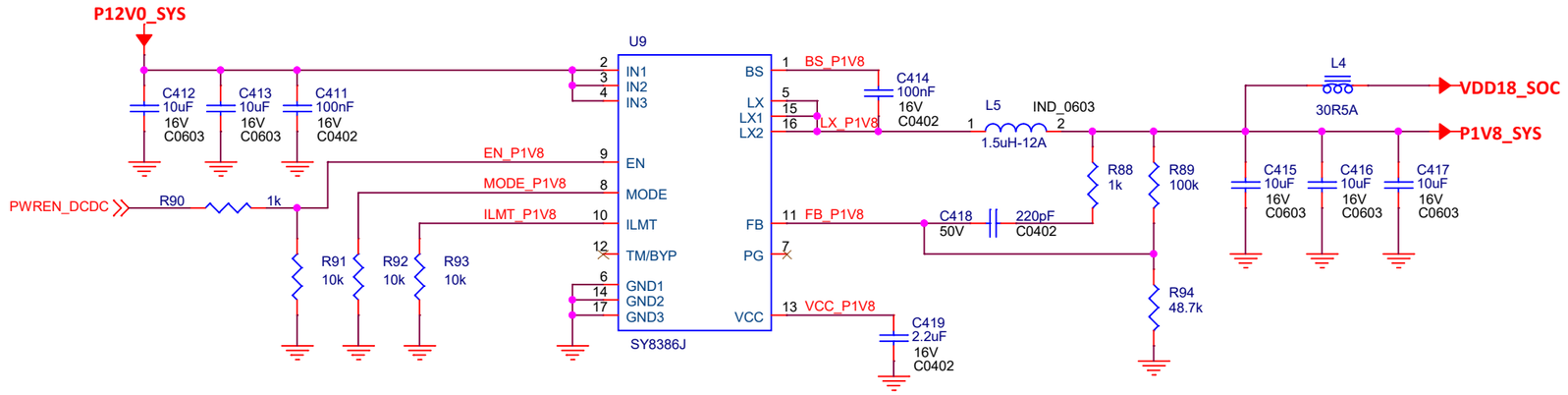
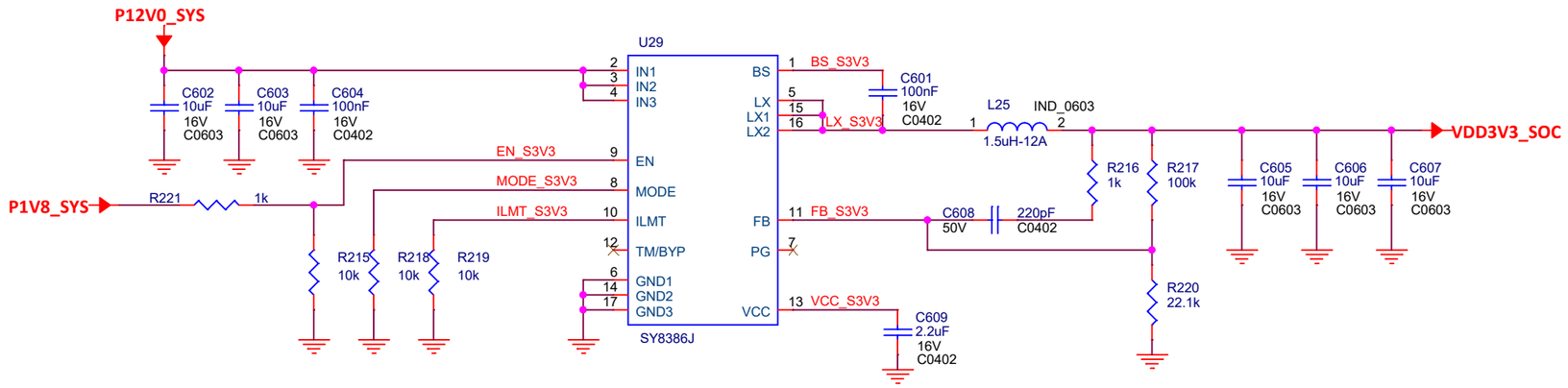
Document Number <Doc>		
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 25 of 29	

Power-DCDC





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Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 26 of 29	

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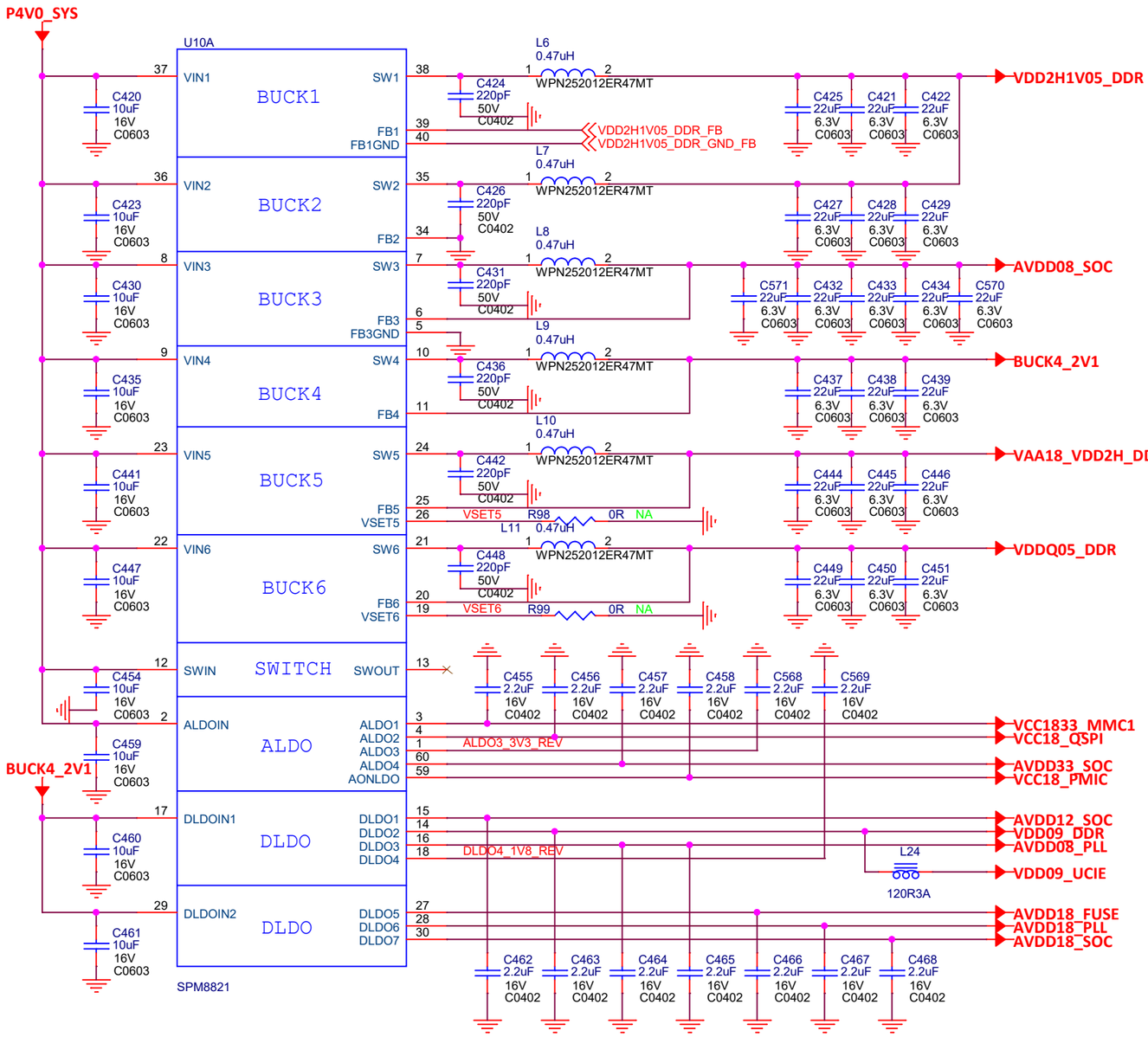

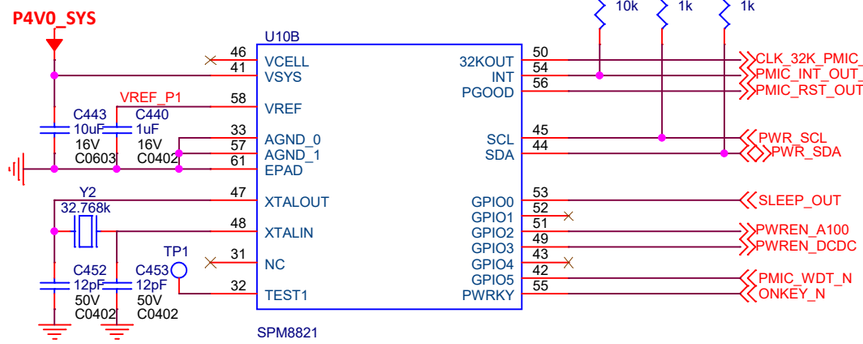

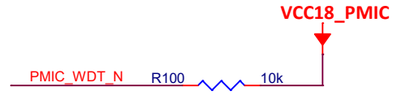

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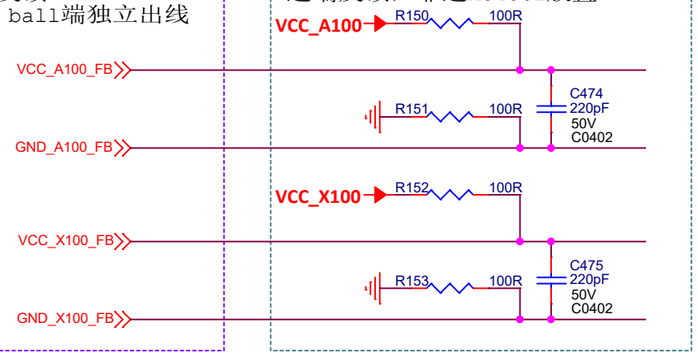
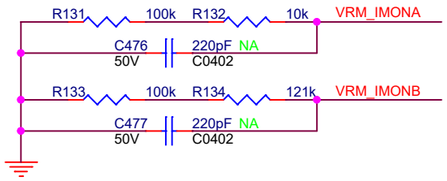
Document Number <Doc>		
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 27 of 29	

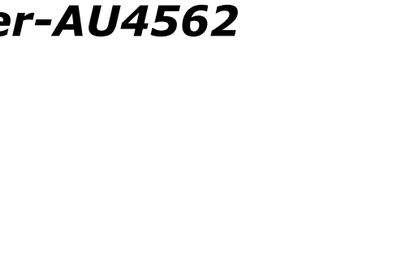
Power-AU4562

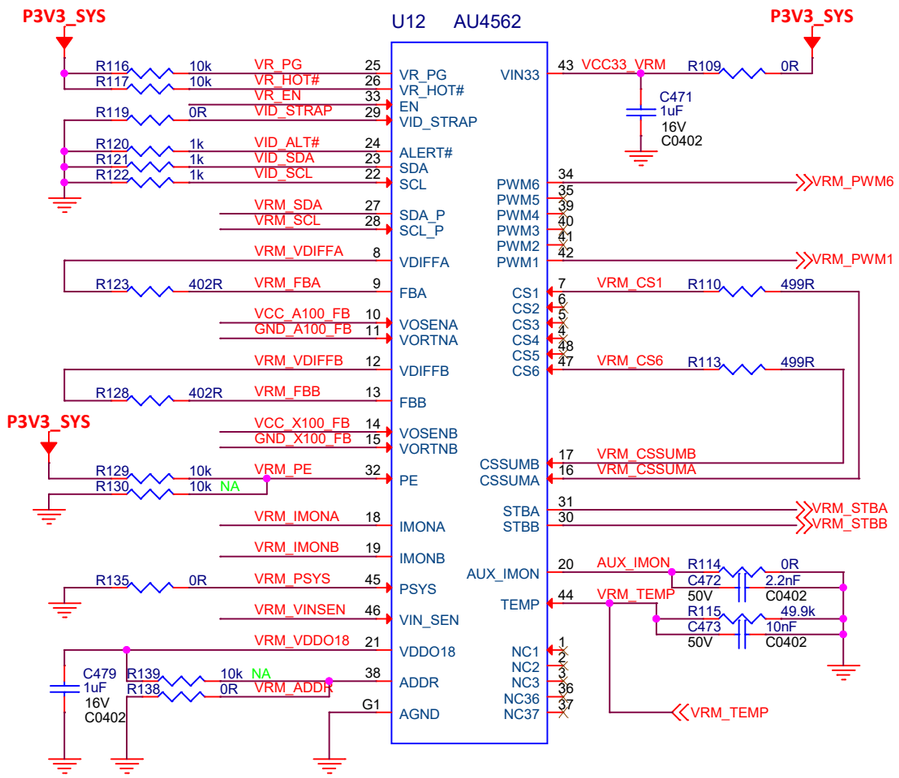
CAD Note:
远端反馈
从K3 ball端独立出线

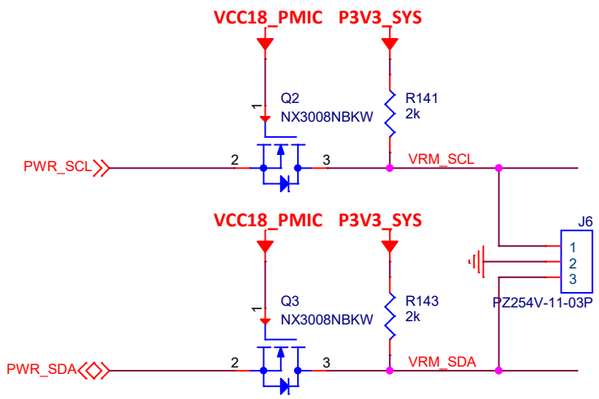
CAD Note:
近端反馈，靠近AU4562放置











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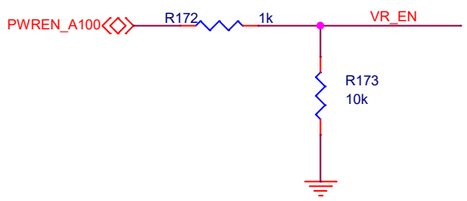

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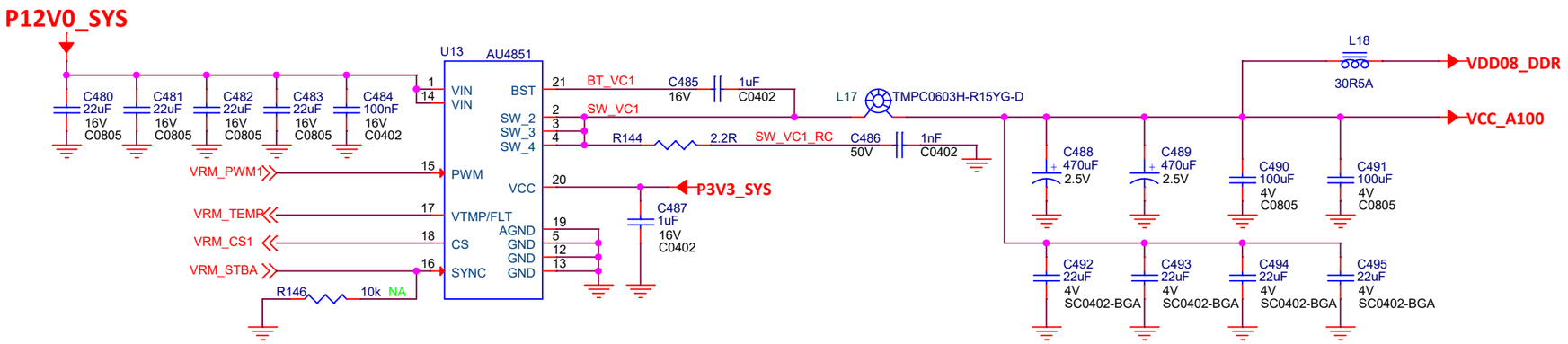
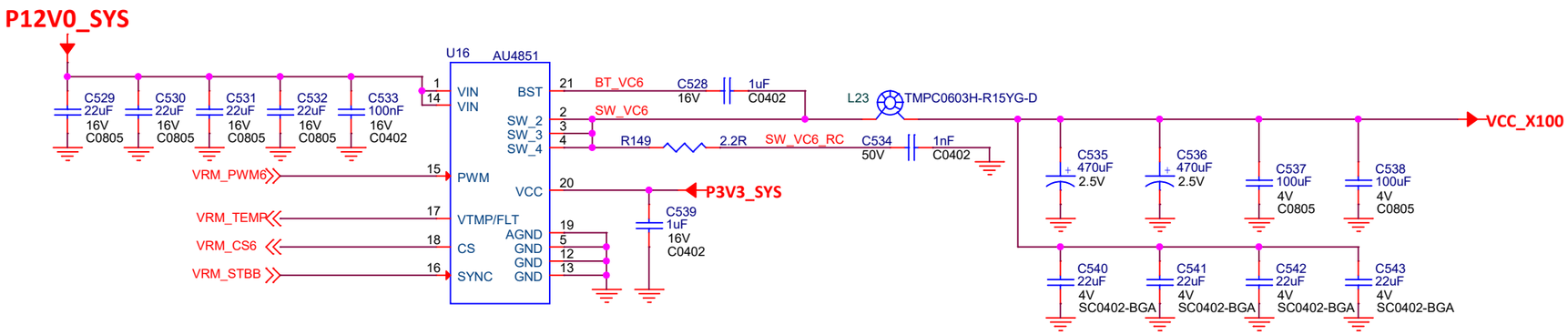
Document Number <Doc>		
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 28 of 29	

Power-AU4851





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Document Number <Doc>		
Size A3	Title <Title>	Rev A
Date: Tuesday, July 21, 2026	Sheet 29 of 29	